

ASTRIUM'S SPACEWIRE BASED LEON PROCESSORS

Session: Components

Short Paper

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ABSTRACT

There are two SpaceWire based processors in Astrium. One is named SCoC3 and one is named MDPA. SCoC3 uses LEON3FT and MDPA uses LEON2FT, both processors are based on SPARC V8 standard.

The main application of SCoC3 is platform while MDPA's main application is payload. The paper describes the different interface modules used to achieve the functionality and also the commercialisation aspects of the two processors.

MDPA (Multi-DSP/micro-Processor Architecture) is a highly integrated System-on-Chip system, which is an advancement on the architecture developed and used on the Inmarsat4 DSP payload. The MDPA is a concept based on a matrix of data processing nodes interconnected using SpaceWire (SpW), with external SpW interfaces to enable connection to other telecommunication, earth observation or science payload subsystem. An MDPA node is in effect a system-on chip which incorporates a highly integrated DVB-S modem co-processor combined with a powerful LEON2FT microprocessor function and relevant interfaces all integrated on the same device. This architecture acts as the controlling unit for the Data Path Subsystem (DPS) within the frame of the next generation of digital telecommunication payloads. Additionally the MDPA concept is laid out for high end control applications or medium rate data processing for earth observation or science payloads.

The 8 SpaceWire interfaces can be used to interconnect several MDPA nodes to a multi-processor configuration. This increases the overall processing performance and enhances the processing redundancy since a faulty node can be replaced by another one. The routing capabilities support the communication of the nodes with low processor interaction. In addition the high number of SpaceWire interfaces allows connection of several remote controlled devices for command and monitoring of subsystems.

The modem function is implemented as hardwired block on-chip. Other devices such as GNSS receivers or reconfigurable co-processors can be used externally and controlled via SpaceWire.

SCOC3 is based on 7 independent AMBA controllers programmed individually by the SPARC processor. They work by using DMA mechanisms to access a specific memory and to free the processor.

They are allocated to CCSDS communications, I/O User communication, Reconfiguration of satellite's system and tests links.

All these SpaceWire links are compliant to the last ECSS standard and are RMAP compatible.