NEXT GENERATION DSP MULTI-CORE PROCESSOR WITH SPACEWIRE LINKS AS THE DEVELOPMENT OF THE "MCFlight" CHIPSET FOR THE ON-BOARD PAYLOAD DATA PROCESSING APPLICATIONS

SESSION: SPACEWIRE COMPONENTS

Long Paper

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ABSTRACT

The paper presents the architecture of the high performance prospective processing SoC with communication protocol SpaceWire as the Next Generation DSP Multi-core Processor for Onboard Payload Data Processing Applications.

DSP Multi-core processor continues processors road map which begins from dual cores processor 0.25-u MC-24R from (chipset "MCFLIGHT") for distributed architectures with SpaceWire interconnections for signal processing and control that is produced by the "ELVEES" company (Moscow). The chip includes the high-performance IP-cores (RISC and DSP), embedded SpaceWire links and high throughput gigabits links, such, as sRIO and SpaceFiber. The planned technology for SOC is 65 – 90 nm RAD HARD CMOS or SOI, that will provide high efficiency (up to tens GFLOPs).

The design and architecture must support Single – Event – Upset (SEU) fault-tolerant. The SpaceWire standard is widely used in asynchronous networks for payload data communication on-board of satellites. The development Multi Core DSP and SpaceWire links integrated on a System on Chip will enable the high performance on-board processing required for future missions.

DSP Multi-core processor SpaceWire links are supported by drivers in Linux that run on the prototype chips. Examples of distributed computer systems (Multi – Ray Satellite Relay, Earth Monitoring with small Satellite Radar with on – board radar images synthesis & compression, Codec for Multi – Media Standard H264/AVC and JPEG-2000 Image compression, Coder (Convolutional, Reed-Solomon) and Decoder (Viterbi, Turbo), which are based on the "MCFLIGHT" chips, illustrate scalable reference structures for distributed signal processing and real-time control systems with SpaceWire interconnections.