

ARCHITECTURE OF THE UNIFIED SYSTEM OF INFORMATION PROCESSING

Session: SpaceWire Mission and Application

Short Paper

Authors 1

Eremeev P. M – the chief of department of Scientific Research Institute "Submicron",

Authors 2

Tarabarov P. A – leading engineer of Scientific Research Institute "Submicron",

Authors 3

Golovlevov D.A. - leading engineer of Scientific Research Institute "Submicron".

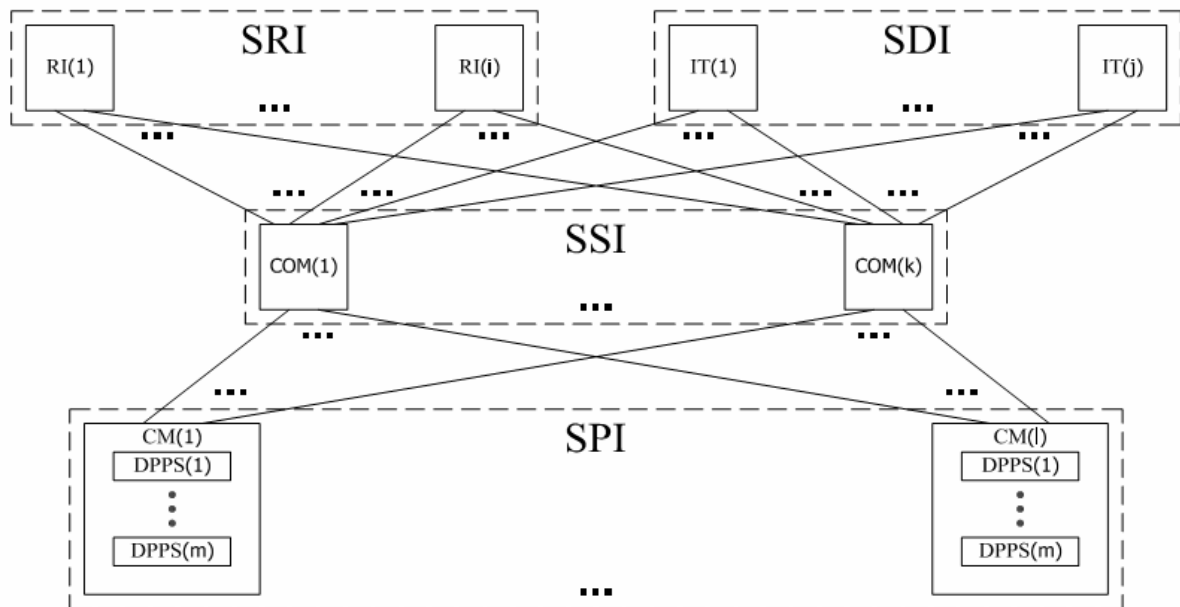
Authors 1, 2 and 3: FSUE Submicron, 124460, Moscow, Zelenograd, 4 South zone, bldg.2

E-mail: author1_epm@se.zgrad.ru, author2_sunland2007@yahoo.com, author3_mastersun1@yandex.ru

Now SpaceWire technology actively **introduce** in modern computing systems (CompS) - control systems (ContrS) and systems of the information processing (SIP) of onboard complexes of aircraft and spacecraft applications.

In structure of any computing system it is possibly to allocate an input-output subsystem, a subsystem of switching (information transfer) and a data processing subsystem. Also in the computing system it is separately possible to allocate a subsystem of management which is the integral component of all above-named subsystems.

Let's consider an example of structure of multimachine system of the information processing (MSIP), presented on drawing 1.



Drawing 1.

MSIP consists of 4 subsystems:

- A subsystem of reception of the information (SRI);
- A subsystem of delivery of the information (SDI);
- A subsystem of switching of the information (SSI);
- A subsystem of processing of the information (SPI).

CM - the computing module,

DPPS - the digital processor of processing of signals,

RI - the receiver of the information,

IT – the information transmitter,

COM – Commutator.

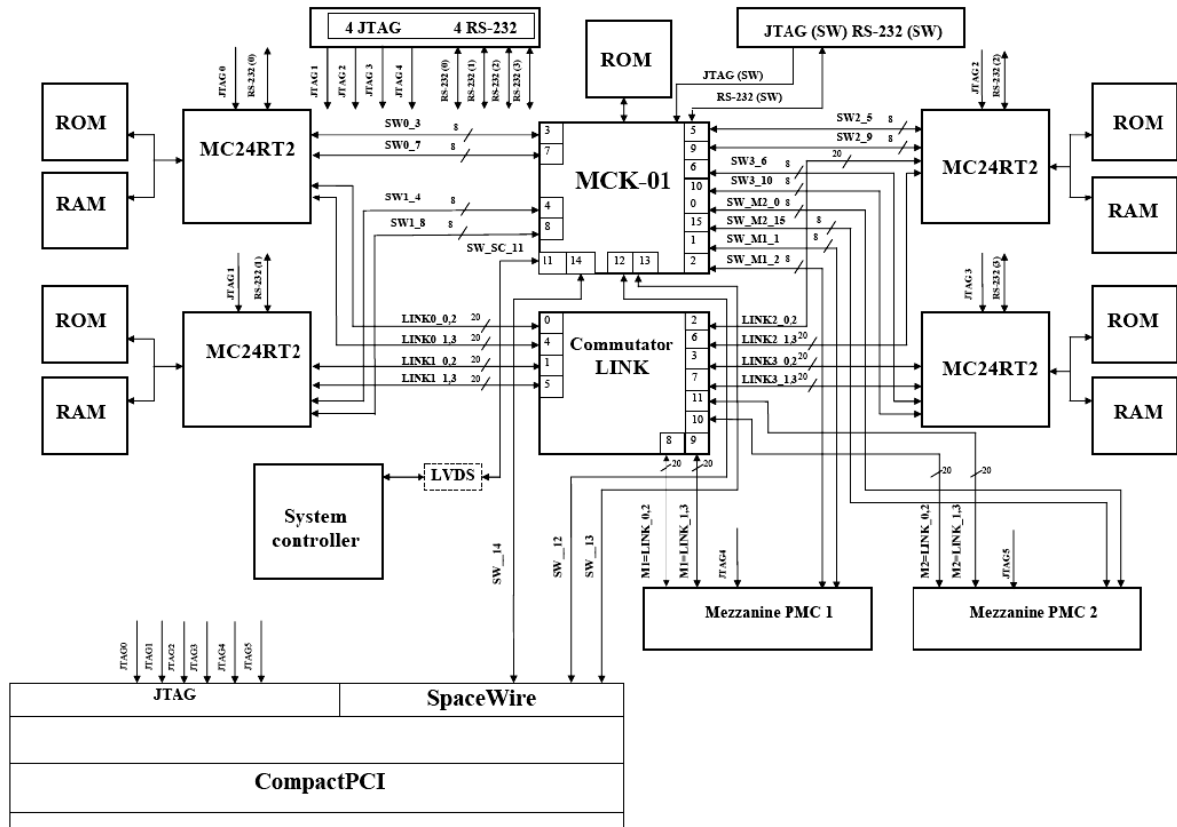
The information transfer, defining work mode and a state of receivers, transmitters, switchboards and processors is direct action of management subsystem.

Frequently the subsystem of management, a processing and information transfer subsystems are constructed on the basis of different interfaces and data transmission protocols. Design of universal architecture of multiprocessors system, in which processing and information transfer subsystems and a management subsystem are based on one interface and the protocol of high-speed consecutive data transmission, will allow to reach on qualitatively new level of multimachine systems design. It will allow:

1. To Increase the general productivity of system at the expense of use of high-speed Space Wire interface in all communication network;
2. To Reduce time of development of hardware maintenance of system at the expense of use at all levels (modular, block, system) the same element base and identical logic and physical principles and design methods;
3. To Simplify and accelerate a development cycle of the general software of system since for transfer of the processed information and the control information is used the same protocol;
4. To Simplify testing and system adjustment.

One of current works in Scientific Research Institute "Submicron" is development of such system on the basis of SpaceWire standard. The basis of this system is the components of Scientific Production Center "Elves": signal microcontrollers of the "Multicore" series - MC24RT2, consist of two SpaceWire ports, and a integrated circuit of the switchboard of SpaceWire interface on 16 ports - MCK-01.

Let's consider block diagram CM which is used for SPI construction. The Block diagram is presented in drawing 2.



Drawing 2.

All four processors MC24RT2 in CM are connected to switchboard MCK-01 with SpaceWire. The controller exercising data control CM (System controller), also is connected to switchboard MCK-01 with SpaceWire. Two ports of the SpaceWire switchboard are connected to sockets for communication CM with SSI. Thus it is visible that switching between of processing information processors, switching of a subsystem of management, and also communication CM with SSI is carried out by one data transmission interface – SpaceWire.

The criteria of fault tolerance put in system, allow it to resist effectively to failures and faults (including to hostile faults) and to carry out detection and identification of appearing faultiness, to carry out reconfiguration at definition of the fault knot, and to carry out safe interrupt systems at impossibility to correspond to the set criteria of fault tolerance.