

A VERSATILE SPACEWIRE CODEC VHDL IP CORE

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Short Paper

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ABSTRACT

Aeroflex Gaisler is specialized in developing IP cores and System-on-chip solutions based on the AMBA on-chip bus. Two SpaceWire IP cores, the GRSPW and GRSPW2, are available for AMBA based systems providing a master interface, advanced DMA and a RMAP target. There is a need for a more basic SpaceWire core with a simpler host interface and this is addressed with the new SpaceWire Codec IP core.

The SpaceWire codec IP core uses the same encoder decoder as in the GRSPW2 IP core. Compared to the GRSPW2 the DMA engines, AMBA interfaces and RMAP target have been removed and replaced with a simpler FIFO based interface. This enables the core to be used in designs without on-chip buses, systems where area is of primary importance and systems where a high degree of customization of the SpaceWire interface is required. For example it is suitable for applications with custom protocols, need for direct dataflow from other cores without using a bus or when other bus interfaces than AMBA are needed.

The core is compatible with several Aeroflex components such as the SpaceWire Physical Layer transceiver, LVDS drivers and RadHard clock buffer.

In addition the core also supports several different SpaceWire input and output schemes compared to other cores. Inputs can be either self-clocking, single data rate (SDR) sampled or double data rate (DDR) sampled. The output can also be either SDR or DDR. Another feature not available in most other cores is the dual-port, which allows a single core to be connected on two different SpaceWire links (not active simultaneously).

The full paper will cover in detail the architecture, host interface, performance, external interfaces and features.