PREPARING THE RASTA SOFTWARE FOR SPACEWIRE BACK-PLANES

Session: SpaceWire Test and Verification

Short Paper

Daniel Hellström, Kristoffer Glembo, Sandi Habinc

Aeroflex Gaisler, Kungsgatan 12, SE-411 19 Göteborg, Sweden

E-mail: daniel@gaisler.com kristoffer@gaisler.com sandi@gaisler.com

ABSTRACT

Aeroflex Gaisler has developed hardware and software for the RASTA (Reference Avionics System Test-bench Activity) that was initiated by the European Space Agency (ESA) to provide a single development platform to reduce the number of different test environments established in technology developments.

The RASTA objectives are to allow the developed technology items to be validated and demonstrated in a flight representative environment, to support mission and spacecraft design and on-board software validation through the project life-cycle by means of a coherent development platform, to maximize reuse of the existing avionics technologies and to be scalable and flexible.

Today RASTA systems are built around on-chip IP cores on the AMBA bus and IP cores accessed over the Compact Peripheral Component Interconnect (cPCI) back-plane. The processor (normally a fault-tolerant LEON3) accesses the various interface cores by means of accesses over the on-chip AMBA bus or through a PCI IP core connecting it to the cPCI back-plane. For pure system-on-a-chip solutions, all communication can also occur over the on-chip AMBA bus. However, most RASTA cPCI boards already include SpaceWire interfaces and connectors on the front-panel, which allows for SpaceWire communication between boards, and this approach can be migrated to future active or passive SpaceWire back-planes.

The crucial parts of the RASTA development platform are the SpaceWire network and the RTEMS operating system with drivers. The key elements implementing the SpaceWire network are the various RASTA boards harboring ASIC or FPGA components implementing the SpaceWire links. Today RTEMS supports RASTA over cPCI and provides means for communicating over SpaceWire; however full support for RMAP and generic models for SpaceWire nodes are missing.

With a new RASTA software layer, other boards can be accessed directly over SpaceWire, without the need to modify the application software. This paper will present an approach to access a complete RASTA system over SpaceWire using RMAP. In the future this approach may be used to replace cPCI communication partially or in whole.

The driver manager in RTEMS allows bus specific routines to be isolated into one location and thereby making software drivers more or less independent of the architecture allowing a high degree of code reuse. From the driver's point of view

hardware discovery, interrupt and driver loading are handled identical to RASTA over cPCI, utilizing the built-in Plug & Play capability. Bus specific routines rely on a RMAP initiator stack that in turn isolates the routines from the specific SpaceWire IP core implementation, thus any SpaceWire codec IP core can be supported.

Using an existing RASTA board with SpaceWire interfaces on the front-panel, the board can act as an RMAP initiator and access RMAP target boards over a SpaceWire network, or be an RMAP target itself, accessible to other RMAP initiators.

The new software is already being used in a separate CCSDS/ECSS telemetry and telecommand FPGA development project to set up, control and transport telemetry frames and receive telecommand frames over SpaceWire using RMAP.

The full paper will discuss in detail the software architecture and design choices made in order to extend the current RTEMS software to support multiple RASTA boards in a heterogeneous SpaceWire network.