SPACEWIRE LINK ANALYSER MK2: A NEW ANALYSIS DEVICE FOR SPACEWIRE SYSTEMS

Session: SpaceWire test and verification

Short Paper

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ABSTRACT

In order to assist with the testing, validation and verification of a SpaceWire system, the STAR-Dundee Link Analyser was developed to seamlessly monitor and record information passing in both directions along a SpaceWire link. A series of triggers could be programmed into the device which, when the monitored traffic satisfied the appropriate conditions, would cease acquisition of link data into the Field Programmable Gate Array (FPGA) embedded memory. The data buffered at the trigger event would then be downloaded to a host Personal Computer (PC) through a USB 2.0 interface.

This paper describes the successor to the Link Analyser: the SpaceWire Link Analyser Mk2. The new device is based on the Xilinx Spartan 6 FPGA, featuring an embedded memory control unit interfaced to 1Gb of external Double Data Rate 3 Synchronous Dynamic Random Access Memory (DDR3 SDRAM). Using the external memory to buffer data allows the SpaceWire Link Analyser Mk2 to capture 2,000 times more characters, data and packets from the SpaceWire link than the existing Link Analyser.

Additionally, the SpaceWire Link Analyser Mk2 adds new features to the Link analyser. Trigger in and out ports allow an external device to issue or register a trigger. An oscilloscope can be connected to the SpaceWire Link Analyser Mk2 to measure, through high impedance buffers, the eye diagram of each link across the termination resistor. A breakout port makes the decoded SpaceWire signals available for viewing with a logic analyser.

These new features make the SpaceWire Link Analyser Mk2 a powerful and invaluable tool for testing, validating and verifying a SpaceWire system.