SPACE-QUALIFIED TRANSCEIVER FOR SINGLE-LINK SPACE WIRE INTERCONNECT

Session: SpaceWire Components

Long Paper

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ABSTRACT

A new interconnect technique utilizing three-level pulses for transmission of data and clock information is presented. This technique is fully compatible with the SW protocol but utilizes only one differential data channel. The second channel normally required for the SW data/strobe link now operates as a redundant line controlled by special circuitry that monitors the integrity of both channels. A transceiver chip that implements a version of the developed technique has been designed and fabricated in a 180*nm* BiCMOS technology suitable for the development of space electronics. Following the successful tests of the transceiver, a SW port with three-level interface has been designed.

1 INTRODUCTION

Performance improvement that is required for the success of future space missions dictates the migration from low-speed parallel to high-speed serial data interconnect interfaces. In contrast with ground-based electronics, achievement of high data transmission rates in space-oriented interconnect systems presents a significant challenge due to tight requirements for their stability in harsh operational conditions. Application of the existing techniques for stability improvement, such as the ones described in [1], inevitably degrades the achievable speed-power performance.

Space plug-and-play avionics is an emerging technology that can alleviate serial data interconnect shortcomings in present-day solutions. It is based on the switching fabric active backplane architecture with robust high-speed serial interfaces. Electrical and/or optical transponders operating with Space Wire (SW) [2], optical SW (SW-Fiber), Fire Wire (FW), or Ethernet/Gigabit Ethernet protocols are required to support the associated high-speed data interconnects.

Unfortunately, the achievable performance of the copper-based SW interconnects is limited by the specific structure of the interface that requires two differential channels per unidirectional link to implement the data-strobe (DS) encoding scheme. Unavoidable channel-to-channel skew accompanied by signal degradation during the transmission process complicates the clock recovery process and prevents system operation at high data rates.

At the same time, the higher flexibility of the electrical SW protocol compared to its optical version makes it extremely attractive for applications in both space-oriented and ground-based systems. This paper presents a novel electrical interconnect technique based on three-level voltage pulses that facilitates the transmission of both data and clock information through one differential channel thus eliminating the channel-to-channel skew problem. As a result, operational speed above 1*Gb/s* can be achieved without modifications of the protocol. In addition, the second differential channel can be used as a redundant connection that increases the fault tolerance of the SW system. Special link integrity control algorithm and circuit have been developed to provide real-time monitoring and activation of the functional link on both transmitter and receiver sides.

The developed interconnect technique has been validated through fabrication of a test transceiver chip with three-level input-output interfaces. The chip was designed on the basis of a special library of fully-differential CML (current-mode logic) cells and functional blocks which utilize SiGe hetero-junction *n-p-n* bipolar transistors (HBT) as active components and poli-Si resistors as loading elements. Those components are available in commercial BiCMOS technologies and offer high speed and natural tolerance to harsh environmental conditions associated with space missions. Following the successful tests of the transceiver chip, a SW port with reconfigurable TL input-output interfaces operating at 1.25Gb/s data rate has been designed within the same library of cells and blocks.

The following sections describe the details of the technique (Section 2), present the design of three-level input/output blocks (Section 3) and SW transceiver chip (Section 4), and discuss the design of a SW port. (Section 5).

2 THREE-LEVEL INTERCONNECT TECHNIQUE

SW protocol relies on the synchronous transmission of two signals, one of which represents the actual data and the other one is a logic XOR function of the data and clock signals. The combination of those signals provides a possibility to reconstruct both data and clock at the receiver side in real time. The same functionality can be achieved with a different three-level (TL) interconnect technique illustrated by Fig. 1 [3].

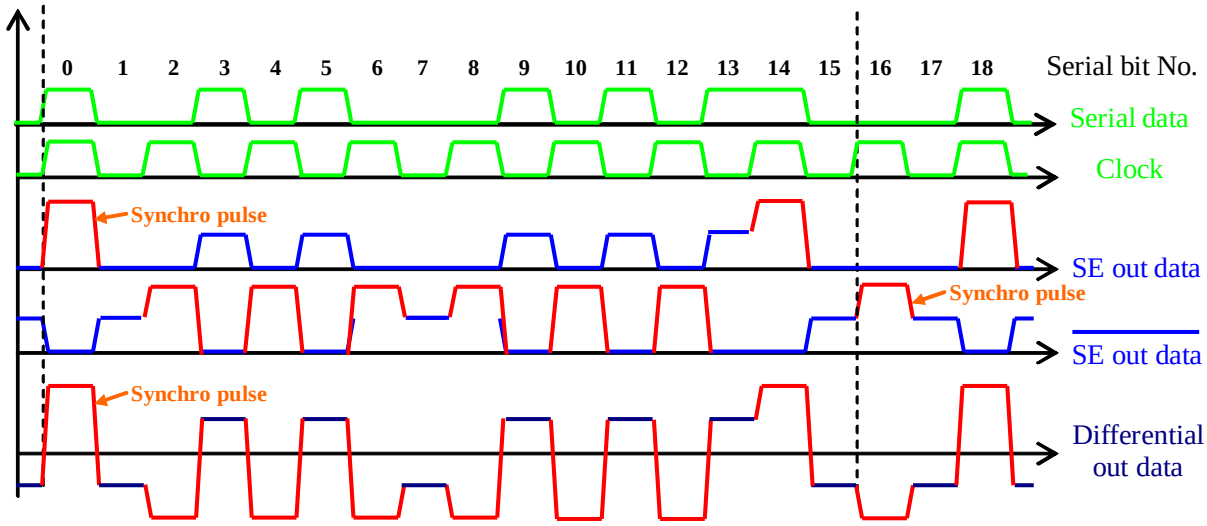


Fig. 1. Timing Diagram of Three-Level Interface.

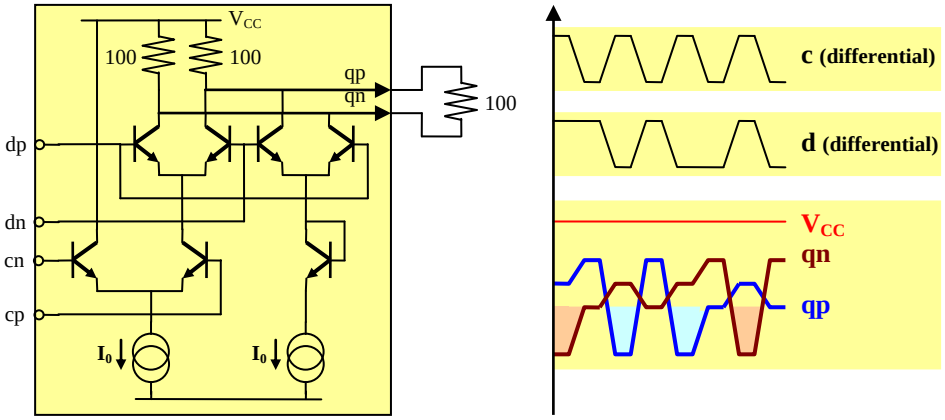
Within this technique, both data and clock information is transmitted through a single differential interconnect line. Prior to transmission, the data is processed by an output three-

level buffer which imposes synchro pulses of increased amplitude onto each odd bit in each single-ended data channel if it has a predefined logic value (either "1" or "0"). Differential signalling guarantees that the synchro pulses are always present in either the direct or the inverted output bit stream as shown in Fig. 1 for synchro pulses represented by higher "1" level. The imposed synchro pulses are retrieved from the input data stream by the receiver's three-level input buffer and converted into a half-rate clock signal required by the SW protocol.

The main difficulties of TL technique implementation are the extraction of single-ended synchro pulses and minimization of the recovered clock jitter primarily associated with the pattern-dependent data jitter.

3 THREE-LEVEL INTERFACE IMPLEMENTATION

The synchro-pulses in TL interface should be represented either by higher levels of logic "1" state or lower levels of logic "0" state. At the same time, the differential bit stream must be compatible with the LVDS (low-voltage differential signalling) electrical interface [4] as defined by the SW standard [2]. To overcome this difficulty, a pseudo-LVDS TL output buffer has been designed. The buffer incorporates a complex logic function of clock "c" and data "d" signals as shown in Fig. 1a. During the periods of negative input clock signal, it generates a logic "1" level equal to "Vcc"-0.4*V* and a logic "0" level equal to "Vcc"-0.8*V* on the external 100*Ohm* load. During the periods of positive input clock signal, the levels are changed to "Vcc"-0.6*V* an "Vcc"-1.2*V* respectively. The resulting signals are shown in Fig. 1b, where filled regions represent the overhead synchro pulses.



a. b.

Fig. 2. TL Output Buffer (a) and Its Signals (b).

The input TL buffer needs to detect the single-ended overhead pulses and convert them into a half-rate clock signal, as well as to process the differential data signals as normal LVDS signals. To perform these functions, the block includes a universal input buffer with high tolerance to common-mode voltage variation [5] that processes the data signals, and a dual comparator that includes two individual comparators connected in series as shown in Fig. 3. The first comparator compares both direct "dp" and inverted "dn" data streams with a threshold voltage "V_{CM}" derived from the input minimum voltage level detected by a peak detector. The resulting signals "q1p" and "q1n" are combined by the logic OR function and compared by the second comparator to the threshold voltage "V_{TH}" derived from the internal

CML logic levels. This dual-threshold technique is self-adjustable to the input common-mode voltage variation within the limits defined by the CML buffer and provides a reliable clock reconstruction within the temperature range from -25°C to 125°C, ±5% of power supply variation, and ±3σ process parameters variation.

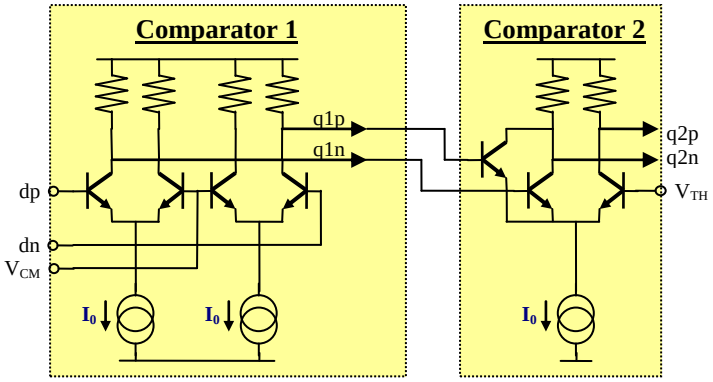


Fig. 3. Dual Comparator.

Computer simulations of the TL interface with realistic package equivalents have proved the acceptable quality of the detected clock signal. The worst-case jitter of the signal does not exceed 0.05UI at the frequency of 1.25*GHz*.

4 TRANSCEIVER TEST CHIP

The discussed TL input/output blocks were incorporated into a complex transceiver chip designed in a commercial 180*nm* SiGe BiCMOS technology. The chip consists of a number of blocks including a multiplexer with TL output interface, a demultiplexer with TL input interface that converts the input data into 40-bit wide parallel output words, and a phase-locked loop (PLL) that uses the reconstructed clock as a reference signal. A microphotograph of the chip is shown in Fig. 4.

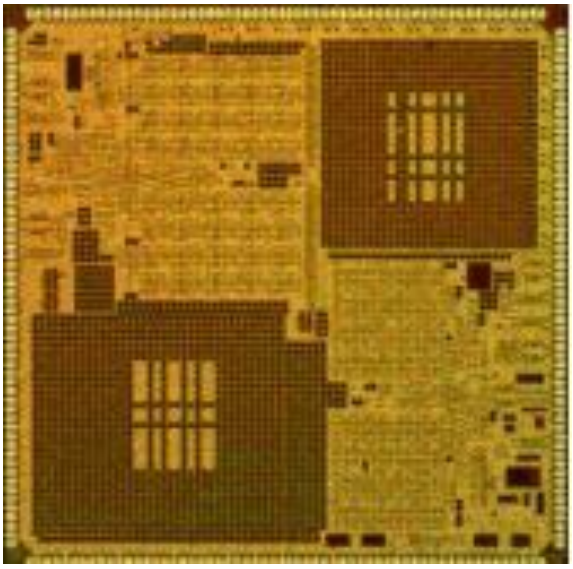
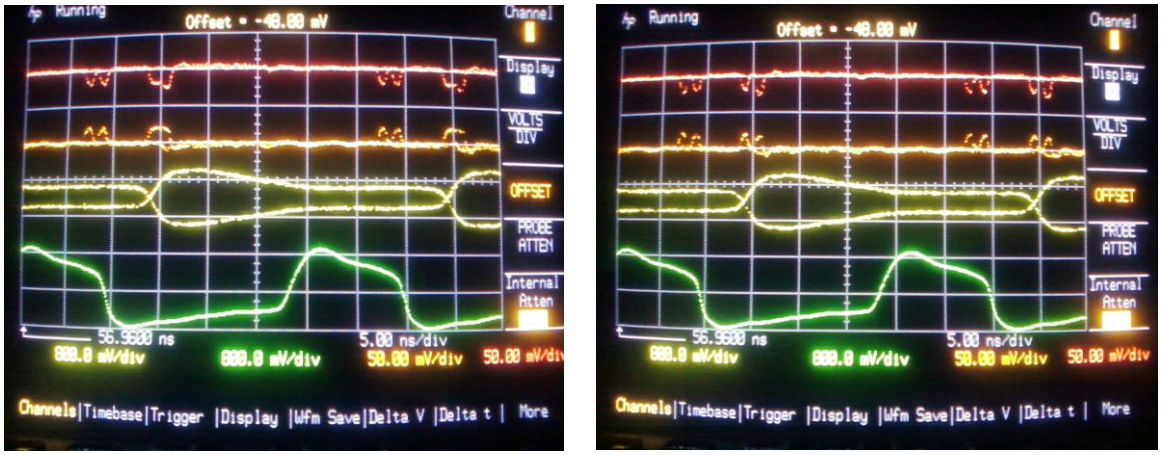


Fig. 4. Microphotograph of the Transceiver Chip.

In this version of TL interface, the overhead pulses are imposed onto each 40-th bit of the data bit stream. The fabricated chip was packaged into a 176-pin TQFN package and tested in a loop mode when the multiplexer's output signal is externally applied to the inputs of the

demultiplexer. The results presented in Fig. 5 demonstrate the transceiver operation in case of equal and opposite data bits overlapping the synchro pulses. These bits are toggling in each 40-bit word. The oscilloscope is triggered by a divided-by-40 clock signal, which causes the double lines on the screen.



a. b.

Fig. 5. Oscilloscope Screen Shots with Equal (a) and Opposite (b) Bits Corresponding to Synchro Pulses.

The top two lines (red and orange) show the direct and inverted TL signals at the multiplexer outputs. The yellow lines show the demultiplexer output signal corresponding to one of multiplexer's toggling input signals. The bottom line (green) shows the synchronized divided-by-40 clock from the demultiplexer's PLL in a lock state.

5 SW PORT DESIGN

Successful test results of the transceiver chip have provided the basis for the low-risk design of the SW port that may serve as a part of a SW switching fabric or other SW devices. The port is designed within the same CML library of cells and blocks. The main parts of the port include a reconfigurable TL transmitter (RCT) with a line integrity control circuitry (LIC) and a reconfigurable TL receiver (RCR) with the same circuitry. The port operates at maximum data rates up to 1.25*Gb/s*. Its block diagram is shown in Fig. 6.

5.1 RECONFIGURABLE TRANSMITTER AND RECEIVER

RCT operates either as a standard SW device where it transmits data and strobe signals through two differential output lines, or as a TL device where it imposes one-bit long synchro pulse on top of each odd bit in both direct and inverted data stream if the corresponding bit has the logic "0" value. The type of the operational mode is defined by control signal "ms2".

Distribution of the output signals among output channels is defined by control signal "ms1T". In the normal SW mode, this switch defines the assignment of data and strobe signals to two output channels. In the TL mode, it works in combination with the "line hardware error" signals "lheT" and defines the active TL channel. Those error signals indicate faulty states of output differential line and are generated by LIC block of RCT that monitors the output lines for short or open conditions.

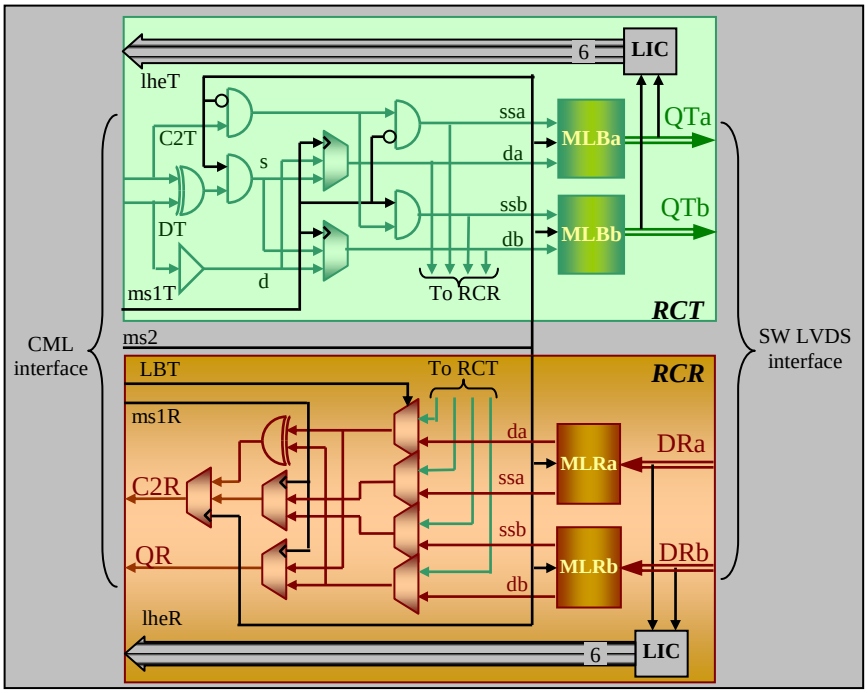


Fig. 6. Block Diagram of SW TL Routing Port.

RCR can operate in the same two modes depending on the state of "ms2" signal. In the normal SW mode, RCR reconstructs the incoming data and half-rate clock signals using the standard XOR logic function. In the TL mode, it extracts the same half-rate clock from the overhead synchro pulses as described in Section 3. RCR also includes the LIC block identical to that of RCT. The "ms1R" signal is used for activation of a certain input channel or identification of data and strobe signals. The optional "loop-back test" mode may be activated by the "LBT" signal. In this case, the transmitter outputs are sent back to the receiver bypassing the SW interface.

5.2 Line Integrity Control

The developed algorithm for the integrity control of the port's input/output lines is based on voltage logic level monitoring. The detectable signal line states of the LVDS-compatible TL interface are reproduced in Table 1, where "dp" and "dn" are the direct and inverted inputs, "qp" and "qn" are the direct and inverted outputs, $\Delta V_L = V^1 - V^0$ is the voltage logic swing, and V_H represents the positive supply voltage.

Table 1. Line State Detection Conditions.

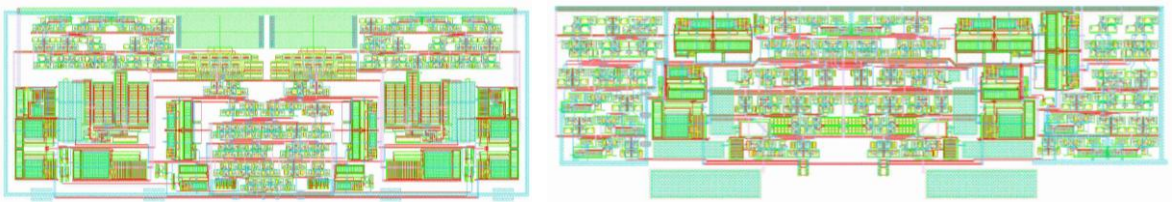
Line State	Input Interface		Output Interface	
	Logic Levels *)	Condition	Logic Levels	Condition
Normal	$V^1=V_H-\Delta V_L$ $V^0=V_H-2\Delta V_L$		$V^1=V_H-\Delta V_L$ $V^0=V_H-2\Delta V_L$	
Broken	$V^1=V_H$ $V^0=V_H-3\Delta V_L$	$V_{dp}= V_{dn}$	$V^1=V_H$ $V^0=V_H-3\Delta V_L$	$V^1=V_H$
Shorted together	$V^1=V_H-1.5\Delta V_L$ $V^0=V_H-1.5\Delta V_L$	$V_{dp}= V_{dn}$	$V^1=V_H-1.5\Delta V_L$ $V^0=V_H-1.5\Delta V_L$	$V_{qp}= V_{qn}$
Shorted to GND	$V^1=V_H/2$ $V^0=0$	$V_{dp}<V_H/2$ $V_{dn}<V_H/2$	$V^1=V_H/2$ $V^0=0$	$V_{qp}<V_H/2$ $V_{qn}<V_H/2$

*) – transmitter levels may be shifted

Looking at Table 1, it is obvious that three independent line controllers are needed at both the transmitter and receiver sides. These circuits are implemented as voltage comparators with threshold voltages $V^{R1}=V_H-\Delta V_L/2-\Delta V_{EF}$, $V^{R2}=(V_H+V_L)/2$, and $V^{R3}=Vcc/2$. They generate a combined error signal corresponding to any of the line faulty condition. This signal can be used by external processor for the activation of the operational interconnect line.

5.3 LAYOUT DESIGN

The layout of the port has been designed using standard cells from the CML library. The top view of RCT and RCR layouts are shown in Fig. 7.



a. b.

Fig. 7. Layouts of RCT (a) and RCR (b).

The simulation of the port's extracted schematic demonstrated its operation at data rates up to 1.25Gb/s. The complete port is ready for the integration into higher-level designs as a macro block. Its implementation in the CML basis makes it directly suitable for space-oriented applications which require tolerance to harsh environmental conditions.

6 CONCLUSIONS

A novel technique for transmission of SW-compatible data and clock information through a single differential interconnect line has been developed and implemented as a transceiver test chip and as a SW routing port. Both designs are made within a special CML library of cells and blocks that is developed in a 180*nm* BiCMOS technology.

Utilization of this technology makes the designs suitable for space-oriented applications which require tolerance to harsh environmental conditions.

Fabrication and testing of the transceiver chip has proven the performance of the developed technique.

A novel algorithm and circuitry for the LVDS line integrity control have been developed. This technique allows for the detection of the line's faulty condition and its replacement with the second line defined in the SW standard but not required for the data transmission through the novel three-level interface.

7 REFERENCES

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