ITAR-FREE FPGA TARGETED CHARACTERISATION OF THE SPACEWIRE CEA IP

Session: SpaceWire Components

Short Paper

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ABSTRACT

The X- and gamma ray telescope ECLAIRs onboard the future mission for gamma ray burst studies SVOM (Space-based multi-band astronomical Variable Objects Monitor) is foreseen to operate in orbit from 2013 on. ECLAIRs will provide fast and accurate GRB triggers to other onboard telescopes, as well as to the whole GRB community, in particular ground-based follow-up telescopes. The ECLAIRs X- and gamma-ray imaging camera (CXG), used for GRB detection and localisation, is combined with a micro-channel X-ray telescope (MXT) for afterglow observations and position refinement. Sub-systems of both instruments interface with the French payload control unit (so called FCU - under CNES responsibility) by mean of SpaceWire links for PUS and CCSDS compliant message exchanges.

1. INTRODUCTION

The SVOM mission being a collaboration between the Chinese and French space agencies specific exportation rules must be fulfilled. In particularly these rules (ITAR, ...) restrict drastically components availability. This is especially critical for microprocessors and FPGAs since most of the manufacturers are in US. In this paper we discuss the implementation of the SpaceWire IP core from CEA on various ITAR-free target candidates. In particularly we present the performances and the implementation specificities for the ATF280 from ATMEL.

2. INSTRUMENT DESCRIPTION

The SVOM payload is divided into two sub-assemblies: one in under the responsibility of the Chinese space agency – so called the Chinese payload – and comprises several instruments such as the Visible Telescope (VT) the Gamma Ray Monitor (GRM) while the second in under the responsibility of the French space agency – so called the French payload – and comprises also several instruments such as the Gamma and X- Ray telescope (ECLAIRs) the Micro channel X-ray Telescope MXT). Figure 1 depicts the overall architecture of the SVOM payload. As shown each 'payload' hosts a control unit in charge of the handling of the instrument covering both command distribution, data acquisition and routing as well as health check functions. Those units interface with the spacecraft by mean of a MIL-STB-1553 bus.

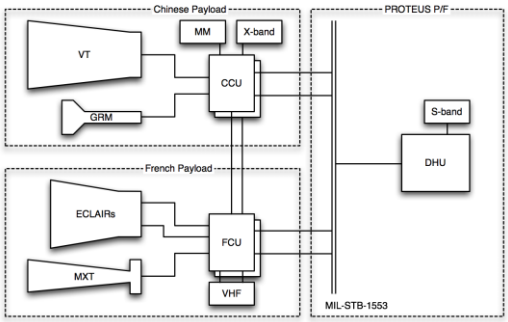


Figure 1 – SVOM block diagram

Lets now focuses on the ECLAIRs instrument whose management is under the responsibility of the CEA. Figure 2 depicts the architecture of this instrument including the camera with both optics ('coded mask'), detector plan ('pixelised' cadmium telluride) and front-end electronics (ELS) the Detector Control Unit (UGD) in charge of control of the camera and finally the Scientific Processing Unit (UTS) in charge of the spatial localisation of the gamma-ray burst either by detecting unexpected source in the field of view ('image trigger') either by detecting an excess in counting rate ('counting trigger'). Both UGD and UTS units communicate with French Control Unit (FCU) for message exchanges. The SpaceWire standard was chosen to implement these interfaces by considering the benefits of using a well-known standard. Thanks to its performances the electrical system is also well optimised since a single link can handle all kind of messages exchanged between the units.

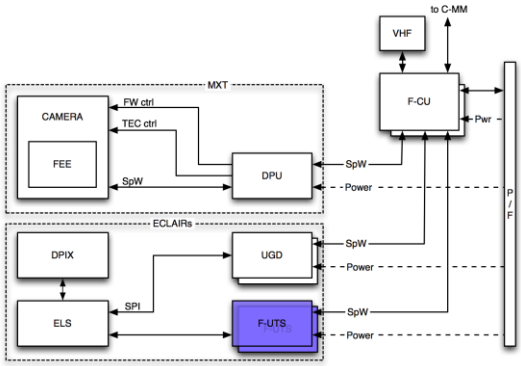


Figure 2 – French payload block diagram

3. THE CHOICE OF THE FGPA

When designing equipments with SpaceWire several options are possible: either to rely on existing implementations of the interface standard in ASIC, as provided by ATMEL or AEROFLEX companies, or either implement an IP core in an FPGA. First option minimizes development risk while the second one offers more flexibility since designers have the opportunity to host other functions of the equipment in the FPGA. It is this second option that was selected for the design of the UTS since the design relies on a LEON processor completed with FPGAs for data interfacing with the camera front end electronics and their pre-processing. Since we already had a lot of experience (HERSCHEL, SIMBOL-X, …) in the implementation of the SpaceWire

standard we felt particularly confident with this choice. Starting from that design concept of the unit the remaining open issue was the selection of the target FPGA. At this time, several years ago, we add various possibilities between XILINX, ACTEL and ATMEL products. XILINX was the best choice at least on paper thank to its performance. But rapidly we had the reject this competitor due uncontrolled risk of failure of the device. Indeed because of the high pin count CGA package the device exhibits a poor reliability under thermal cycling condition. Next choice was the RTAX family from ACTEL, and again we had to reject it not for technical reason this time but due to exportation limitations (all the parts of the family are ITAR classified). Not classified parts from ACTEL were still available (RTSX family), but limited number of cells and lack of memory were not compliant with the requirements, except eventually for the implementation of the SpaceWire. Finally the only remaining solution was the ATF280 from ATMEL manufactured in Europe and therefore free of any exportation constraint, re-enforced by classification end 2009 of the ACTEL RTSX family.

4. FPGA DESCRIPTION

The ATF280 is a radiation hardened SRAM-based reprogrammable FPGA featuring 280K equivalent ASIC gates and re-programmability. It contains 14400 logic blocks – cells- with 2 x 3 inputs and a register element, a D-type flip-flop, with programmable clock and reset polarities. Additionally it features 115 Kbits of dual-port RAM called FreeRAM^{TM}. The FreeRAM^{TM} is SEU hardened and is made of 32 x 4 dual-ported RAM blocks and dispersed throughout the array. The ATF280 has been especially designed for space application by implementing hardened cells and permanent self-integrity check mechanism (300 krad max TID and 80 MeV LET_{th}). It is available in two space-qualified packages: MCGA472 and MQFP256 packages offer respectively 324 I/Os and 166 I/Os for user application. The FGPA is available either in QML-Q and V or in ECSS quality grades.

5. IMPLEMENTATION OF THE SPACEWIRE CEA IP

The implementation of the IP is achieved by mean of the software tools provided by ATMEL. It includes a VHDL synthesiser (Precision RTL 2008a1.11 OEM_Atmel from MENTOR) a router (Atmel Figaro IDS V9.0.2) and a programming tool (SpaceProgrammer v 4.0. from ATMEL). Design verification is achieved with the VHDL simulator ModelSim (from MENTOR).
The implementation of the SpaceWire CEA IP is done ‘as it is’ and only few compiler directives shall be selected. The test set-up includes the Aerospace Development Kit (ADK) evaluation board dedicated to ATMEL space qualified processors and FPGAs with the ATF280 mezzanine board plugged-in. The ADK hosting the SpaceWire CEA IP is connected to a PCI acquisition board (PCI^{4SpW} from Skylab – Toulouse). Specific software permits the sent and the reception of data to the destination node as well as to check the link status.

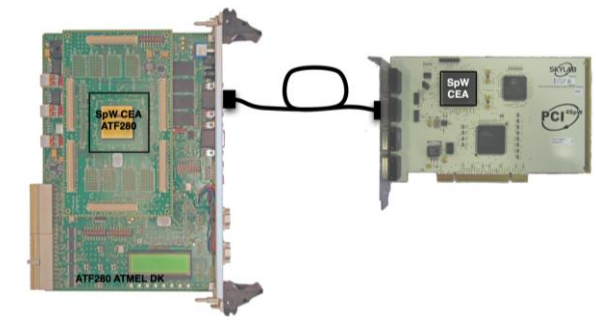


Figure 3 – Test set-up

6. RESULTS

Various configurations have been evaluated in the target FPGA. The first one consists in connecting the transmitter inputs (‘Tx’ block) to the receiver outputs (‘Rx’ block) as simply as possible (see figure 4-a). The second one consists in the implementation of a command decoder and a counter along with the IP. On reception of a ‘start / stop command’, the counter starts or stops counting and its current content is continuously sent back (see figure 4-b). This second configuration is more representative of real designs where the SpaceWire IP is supposed to interface with equipment specific functions (i.e. data processing). A third configuration was also tested (see figure 4-c) but results were not reproducible and therefore no result are reported in the present paper.

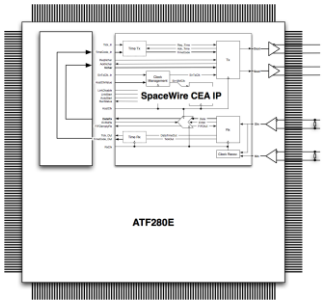
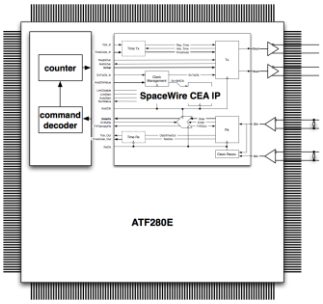
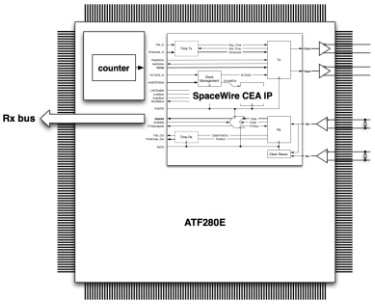


Figure 4-a: Configuration 1



-b: Configuration 2



-c: Configuration 3

Configuration 1

Frequency	10 MHz	40 MHz	100 MHz	120 MHz	140 MHz
Rx	OK	OK	OK	OK	FAIL
Frequency	10 MHz	30 MHz	40 MHz	50 MHz	100 MHz
Tx		OK			

IDS report:

```
*********************************************
Device Utilization for ATF280E-MCGA472
*********************************************
Resource                Used    Avail     Utilization
-----------------------------------------------
IOs                     9       308       2.92%
Combinational Cells     576     14400     4.00%
Sequential Cells        198     14400     1.38%
```

Configuration 2

Frequency	20 MHz	50 MHz	100 MHz	120 MHz	140 MHz	160 MHz
Link connected	OK	OK	OK	OK	OK	OK
Data received	OK	OK	OK	OK	ERRORS	NO DATA

7. CONCLUSION

These early results show promising performance of the SpaceWire CEA IP in the ATMEL ATF280 FPGA. Performance required for the ECLAIRs instrument – 10 MHz links - is already satisfied. Further tests are on-going and unpredictable operation of configuration 3 will have to be understood.