

GR712RC – A MULTI-PROCESSOR DEVICE WITH SPACEWIRE INTERFACES

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Short Paper

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ABSTRACT

The GR712RC device is a first of its kind, offering the space community powerful multi-core processor capability in combination with multiple RMAP [6] enabled SpaceWire links [5]. The device is highly configurable and can operate in many different applications, ranging from platform control to payload processing.

GR712RC DUAL CORE LEON3-FT

1.1 OBJECTIVES

The GR712RC device has been designed to provide high processing power by including two LEON3FT 32-bit SPARC V8 processors [7], each with its own high-performance IEEE-754 compliant floating-point-unit and SPARC reference memory management unit. This high processing power is combined with a large number of serial interfaces, ranging from high-speed links for data transfers to low-speed control buses for commanding and status acquisition. The GR712RC can be utilized in symmetric or asymmetric multiprocessing mode. The processors provide hardware support for cache coherency, processor enumeration and interrupt steering.

1.2 FEATURES

The main functions of the GR712RC device are:

- 2 x LEON3FT 32-bit SPARC V8 Processor with
 - IEEE-754 High-performance Floating Point Unit (FPU)
 - SPARC V8 Reference Memory Management Unit (MMU)
 - 4x4kByte Instruction Cache, 4x4kByte Data Cache
 - Branch prediction
- Debug Support Unit with JTAG Debug Interface
- 6 x SpaceWire links, of which two with RMAP
- 10/100 Mbit/s Ethernet MAC
- Redundant Mil-Std-1553B BC/RT/MT (A/B)
- 2 x CAN 2.0B
- I²C and SPI interfaces
- 8 x Timers, 6 x UARTs, Interrupt Controller, General Purpose Input/Output
- CCSDS/ECSS Telemetry and Telecommand [1][2][3][4]
- 192 kByte On-chip SRAM with ECC
- Memory controller for SRAM/PROM/SDRAM/IO with BCH and RS protection

The variation in interfaces allows different systems to be implemented using the same device type, which simplifies parts qualification and procurement. It also brings cost reductions to software development since the core functionality can be reused from application to application, only changing the drivers for the interfaces. Due to the high amount of peripherals and a limited number of pins there is an I/O switch matrix that controls which peripheral is connected to each pin.

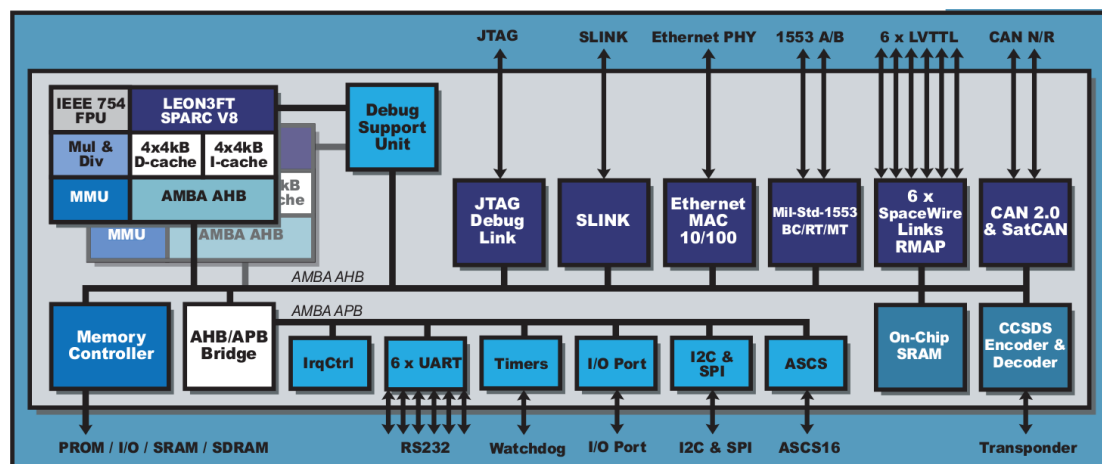


Figure: GR712RC block diagram

The clock gating unit can turn off the clock for each major peripheral thus lowering power consumption considerably. The processor clock is automatically turned off when a processor is in power down mode. The FPU is clock gated when floating point operation is disabled or when the corresponding processor is powered down.

1.3 PERFORMANCE

The expected performance of the GR712RC device at 100 MHz system clock frequency is approximately 250 Dhrystone MIPS. The expected speed of the SpaceWire links is above 200 MBPS.

1.4 TECHNOLOGY

The GR712RC is fabricated at Tower Semiconductors Ltd., using standard 0.18 μm CMOS technology. It employs Rad-Hard-By-Design methods from Aeroflex Gaisler and Ramon Chips. As a preparation for this development, a first ASIC silicon prototype, the GR702RC, with integrated processor and SpaceWire interfaces has been successfully manufactured, validated and undergone radiation testing. The final GR712RC device is expected to be latch-up free, be fully protected against single event upsets in registers and memory, and tolerate a high total ionizing dose.

To allow flexibility and possibility for fault-containment, the Low-Voltage Differential Signaling (LVDS) buffers required for the SpaceWire interfaces need be implemented off-chip using standard components.

1.5 PACKAGING AND AVAILABILITY

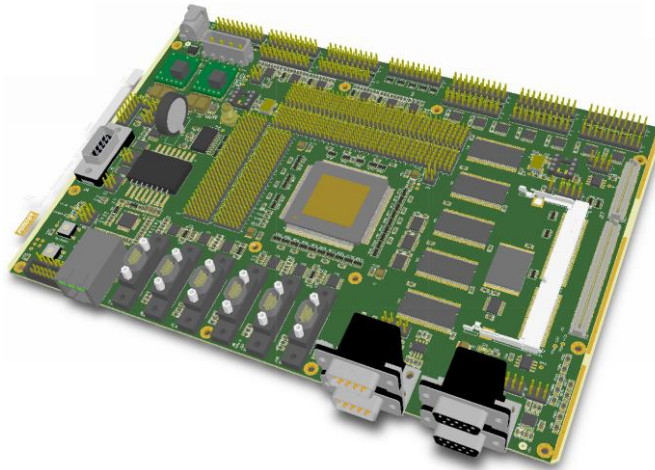
GR712RC will be packaged in a 240-pin Ceramic Quad Flat Package (CQFP) meeting high pin count, low die size, manufacturability and testability requirements.

The GR712RC will be available as engineering samples in August 2010. Space qualified parts will be available in first half of 2011. Prototyping and evaluation is possible using the GR712RC development board.

GR712RC DEVELOPMENT BOARD

In order to provide a platform for customers to begin developments using the GR712RC device, Aeroflex Gaisler provides a GR712RC development board. The board comprises a custom designed PCB in Compact PCI 6U format which can be used either stand alone or inserted into a CPCI rack.

The board has interfaces for all peripherals and 8 MByte of SRAM (with check-bits), 8 MByte of Flash PROM, and a standard SDRAM SODIMM socket. Each pin in the I/O switch matrix is configured with a jumper. All the interfaces are conveniently



located on the front side of the board, allowing easy access to a CPCI front-panel.

Figure: GR712RC development board

MULTIPROCESSOR NETWORKS OVER SPACEWIRE

The multiple SpaceWire links allow the GR712RC device to be used in multiprocessor applications, providing two high-performance processors in each node.

The onboard payload reference network is a marriage between the high-speed backbone SpaceWire network and the low-speed spacecraft control bus based on CAN or Mil-Std-1553B. The SpaceWire network is well suited for bulk data transfers, whereas the CAN or Mil-Std-1553B bus is suited for control and sensor acquisition tasks. The need to bridge the networks can be seen from several perspectives.

The GR712RC can be integrated in the Instrument Controller Unit (ICU) which acts as the payload data processor and mainly receives payload data from instruments and produces processed data to be downlinked. The main data communication is performed via the SpaceWire network. The ICU is however controlled and monitored via the CAN or Mil-Std-1553 bus from the On-Board Computer (OBC). The GR712RC then acts as a remote terminal which is being managed by the OBC.

Alternatively, the GR712RC can be integrated in the OBC. Since the OBC acts as the network manager on the CAN network, the CAN controller must carry capability such as node management and time distribution. The same approach applies to the Mil-Std-1553B bus. The OBC also communicates or manages the SpaceWire network via SpaceWire links.

As can be seen from the two above application scenarios, the capabilities of the GR712RC is not limited only to support the CAN/Mil-Std-1553B buses in an ICU, but will also allow its usage in the OBC. This will reduce development costs since the same device is used in both payload and avionics. This will also promote the usage of hybrid SpaceWire and CAN/Mil-Std-1553B networks. To support both applications, the GR712RC facilitates sufficient processing power as well as suitable interfaces.

To bring the concept a step even further, one could envisage applications in which the GR712RC actually replaces the signal processor in an ICU or instrument. The processing capacity of the GR712RC then needs to be at least as great as can be expected for current monolithic signal processor devices. Such a concept would provide great savings in terms of power and board area, since a single device with some external memory would be sufficient to form the signal processing core.

The ultimate step would be to use the GR712RC processing capacity and number of SpaceWire links to take on the same role as the Transputer [9] used to have. This requires that the on-chip processor provides adequate floating point capacity. At the same time, the architecture is to be scalable and allows operation under low power conditions by means of reducing the clock frequency and the use of few external memory devices. It is not clear if there will be a follow on for the current European digital signal processor, as 32-bit DSP manufacturers are not numerous and are in general not interested in licensing their technology for a niche sector like space. The GR712RC can fill this gap since being sufficiently performant.

Examples of how the GR712RC device can be used to build a fault-tolerant SpaceWire computer is discussed in [8].

CONCLUSIONS

The GR712RC device brings multi-processing to avionics and payload applications, increasing the processing performance compared to existing solutions, without consuming board real estate or demanding complex memory implementations.

The GR712RC development board has been designed to support initially stand alone operation, but also to fit into future architectures where inter-board communication is realized through active or passive SpaceWire backplanes.

REFERENCES

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