ECSS TM/TC COMPONENT WITH SPACEWIRE RMAP INTERFACES

SpaceWire Components

Short Paper

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ABSTRACT

Traditionally the implementation of telemetry encoders and telecommand decoders for space has been made in hardware, at least for the last two decades. With the availability of more processing power (e.g. LEON3-FT - 32-bit fault-tolerant SPARC V8 processor), more of the encoding and decoding tasks can be moved to software, allowing flexibility for adapting the system to on-going standardization efforts. Combining the above approach with the use of SpaceWire Remote Memory Access Protocol (RMAP) [13] results in an interesting component and software architecture.

TELEMETRY AND TELECOMMAND BACKGROUND

The return of software-based decoders in space was made in late 2009 with the launch of the European technology demonstrator satellite PROBA-2. The telecommand decoder implementation was made partially in hardware (the lower protocol layers) and partially in software (the higher protocol layers). A telemetry encoder based on similar principals has been developed, and both are being used in several on-going projects in the frame of the ESA Reference Avionics System Testbed Activity (RASTA). Both designs have been used to form the basis of a novel Field Programmable Gate Array (FPGA) TM/TC design.

ARCHITECTURE

1.1 TECHNOLOGY

The ECSS and CCSDS compliant TM/TC flight device FPGA has implemented in the anti-fuse RTAX2000S technology from Actel [18], which is radiation hard, latch-up immune, and has single-event upsets protected flip-flops. The on-chip (and off-chip) memories are protected against single-event upsets by means of BCH-based EDAC.

1.2 FUNCTIONALITY

The telemetry and telecommand concept is based on implementing the associated protocols partly in hardware and partly in software. The lower layers, such as physical layer and the channel coding sub-layer, are implemented in hardware, whereas high levels such as data link – protocol sub-layer are implemented in software. To provide the user with emergency capabilities, certain functions are implemented solely in hardware, for example pulse commands.

The TM/TC FPGA device features the following functions:

- CCSDS / ECSS compliant Telemetry encoder [2][8][9]:
  - Virtual Channels implemented in software, via a SpaceWire RMAP I/F
  - Virtual Channels implemented in hardware, via two SpaceWire RMAP I/Fs [3]
  - Reed-Solomon and Convolutional encoding in hardware [1][7]
- CCSDS / ECSS compliant Telecommand decoder [5][10]:
  - Multiple Virtual Channels implemented in software, via a SpaceWire RMAP I/F
  - One Virtual Channel implemented in hardware, with parallel pulse commands
  - Start sequence search and BCH decoding in hardware [4]

The mix between hardware and software implementation carters for a safe and sound system at the same time as flexibility is provided to support upcoming standards.

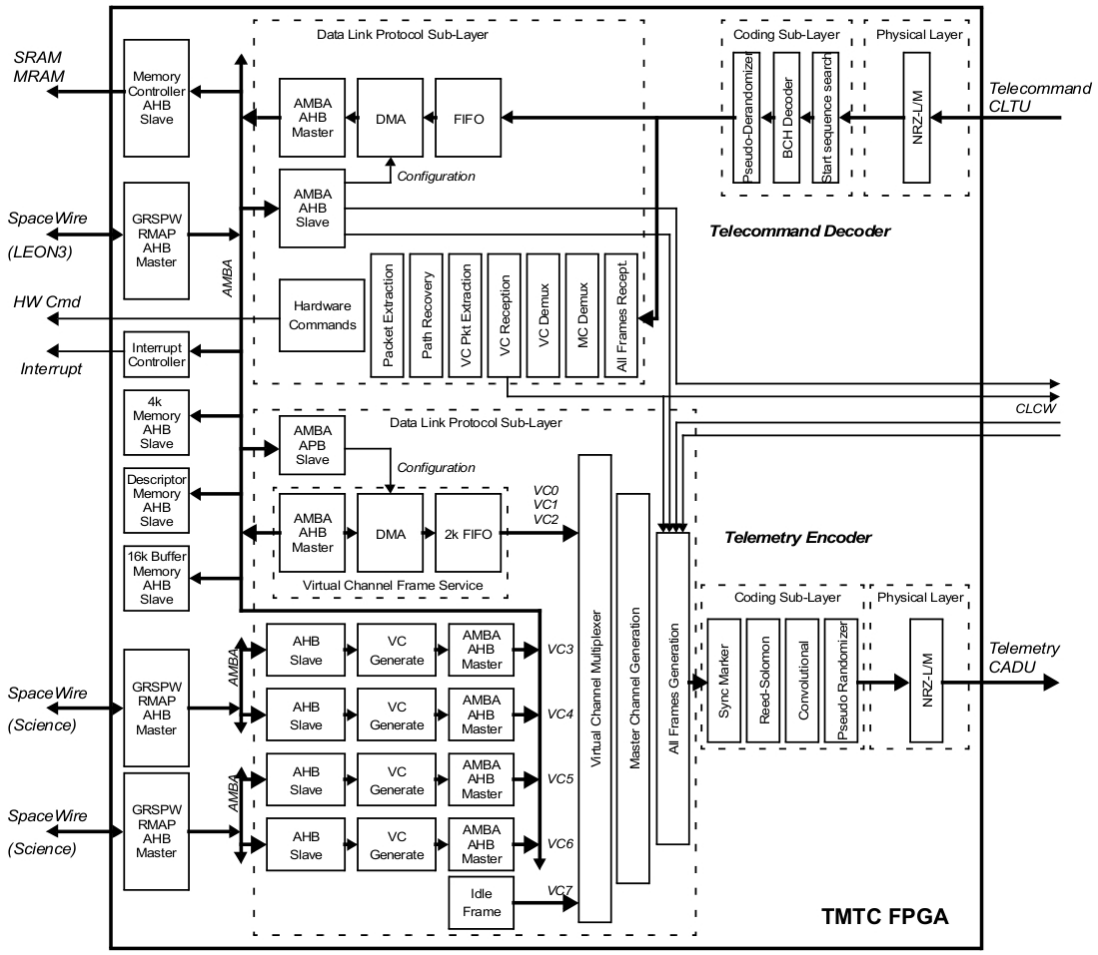

Figure: TM/TC FPGA block diagram

SPACEWIRE RMAP USAGE

1.3 INTERFACES

The main interfaces towards the TM/TC FPGA are three independent SpaceWire links [11] that implement Remote Memory Access Protocol (RMAP) [13] completely in hardware. The TM/TC FPGA implements three RMAP targets. This allows an RMAP initiator to directly access the various functions inside the TM/TC FPGA by means of

RMAP read and write commands sent over SpaceWire to the TM/TC FPGA. The various cores in the TM/TC FPGA are thus memory mapped as seen from a SpaceWire RMAP initiator. A SpaceWire initiator can be any unit capable of sending and receiving SpaceWire packets, with the RMAP protocol implemented in software.

1.4 COMMUNICATION

The novelty of this device is that the communication between the telemetry and telecommand system and on-board computer, as well as payload, is done by means of RMAP over SpaceWire links. Via RMAP read and write commands the device status can be observed and it can be controlled in a safe (verified-write command) and standardized way (ECSS standard).

For software telemetry and telecommands, complete transfer frames can be moved between the device and on-board computer. For hardware telemetry, complete Space Packets can be sent from payload to the device. The RMAP target implementation in the TM/TC FPGA requires no local processor, simplifying the design and releasing logic resources. The CCSDS / ECSS telemetry software stack [2][8] and telecommand software stack [6] are executed on an external processor and the communication is handled via RMAP.

The external processor does not need to implement RMAP in hardware. An RMAP initiator can be any device that can generate standard SpaceWire packets. The RMAP command is just a SpaceWire packet sent from the processor using its SpaceWire core. The RMAP response is just a SpaceWire packet sent from the TM/TC FPGA to the processor. A complete RMAP initiator software stack has been implemented for the RTEMS real-time operating system.

DEVELOPMENT HARDWARE

The TM/TC FPGA has been prototyped using existing development, mezzanine and accessory boards:

- GR-CPCI-AX2000 Development Board
- GR-TMTC-MEZZ Mezzanine Board
- GR-TMTC-ADAPTER Accessory Board
- GR-MRAM Mezzanine Board

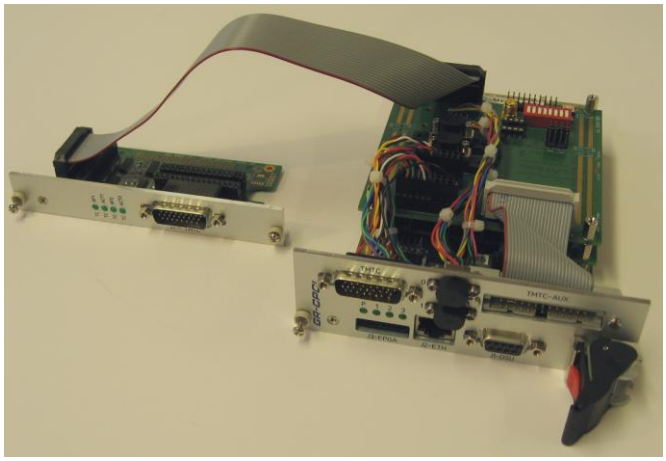

Figure: TM/TC FPGA development boards

CONCLUSIONS

The TM/TC FPGA design and development hardware has been tested and validated with the target software and has been delivered to the first customer. The various IP cores [14][15][16] used to implement the FPGA can be used in other designs, allowing custom implementations to be created. The use of RMAP over SpaceWire as the main communication channel has been proven to work efficiently.

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