SPACE-QUALIFIED 1.25GB/S NANO-TECHNOLOGICAL TRANSPONDER FOR SPACE WIRE OPTICAL/ELECTRICAL INTERCONNECTS

Session: SpaceWire Components

Long Paper

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ABSTRACT

A space-qualified SW-compatible and Ethernet-compatible Transponder ASIC with 1.25*Gb/s* LVDS serial input/output interfaces and 10-bit wide 125*Mb/s* CMOS parallel input/output interfaces is presented. The chip with power consumption below 150*mW* utilizes a special SCL library of cells and blocks including proprietary extra low-power LVDS buffers. It features a clock multiplication unit on the transmitter side and a clock and data recovery block on the receiver side. Three built-in test modes provide a possibility for a detailed self-testing of the part. The Transponder fabricated in a 90*nm* CMOS technology and packaged in a 64-pin QFN plastic package has demonstrated a reliable operation during laboratory tests.

1 INTRODUCTION

Performance improvement that is required for the success of future space missions dictates the migration from low-speed parallel to high-speed serial data interconnect interfaces. In contrast with ground-based electronics, achievement of high data transmission rates in space-oriented interconnect systems presents a significant challenge due to tight requirements for their stability in harsh operational conditions. Application of the existing techniques for stability improvement, such as the ones described in [1], inevitably degrades the achievable speed-power performance.

Space plug-and-play avionics is an emerging technology that can alleviate serial data interconnect shortcomings in present-day solutions. It is based on the switching fabric active backplane architecture with robust high-speed serial interfaces. Electrical and/or optical transponders operating with Space Wire (SW) [2], optical SW (SW-Fiber), Fire Wire (FW), or Ethernet/Gigabit Ethernet protocols are required to support the associated high-speed data interconnects.

Unfortunately, the achievable performance of the copper-based SW interconnects is limited by the specific structure of the interface that requires two differential channels per unidirectional link to implement the data-strobe (DS) encoding scheme. Unavoidable channel-to-channel skew accompanied by signal degradation during the transmission process complicates the clock recovery process and prevents system operation at high data rates.

All electrical interconnects are also susceptible to EMI, which presents a significant danger to spacecraft's electronics. Taking into consideration the described limitations, one of the most suitable solutions is the replacement of electrical links with fiber-optical lines. This approach requires the development of an electrically DC balanced transponder that interacts with standard optical modules on the high-speed side and standard data processors (e.g. FPGA) on the low-speed side.

This paper presents a design of such transponder with the characteristics detailed in Table 1:

Table 1. System Specifications.

Parameter	Value	Units	Comments
Data encoding type	8B10B		
Parallel interface size	10+1	bits	Data and Clock
Parallel interface type	1.8*V* CMOS		
Low-speed data rate	125	*Mb/s*	
Serial interface type	LVDS		Low-voltage differential signalling [3]
High-speed data rate	1.25	*Gb/s*	
Power supplies	1.8	*V*	±5%
Power consumption	<150	*mW*	

The following sections describe the transponder architecture (Section 2), explain the utilized library-based design approach and discuss the library structure (Sections 3.1), describe chip design (Section 3.2) as well as its fabrication and testing (Section 4).

2 TRANSPONDER ARCHITECTURE

The required functionality can be naturally achieved in a 2-channel serializer/deserializer (SERDES) system shown in Fig. 1. To process the 8B10B data, SERDES includes a transmitter channel (Tx, green blocks in Fig. 1) with 10-to-1 MUX CMU (multiplexer with internal clock multiplication unit), CMOS input parallel interface (CMOS IB), 2-bit FIFO (first-in-first-out), and an LVDS output buffer (OB); as well as a receiver channel (Rx, brown blocks in Fig. 1) with CDR (clock and data recovery unit), 1-to-10 DMUX (demultiplexer), LVDS input buffer (IB), and CMOS output parallel interface (CMOS OB). Two internal phase-locked loops (PLLs) in CMU and CDR synchronize the transponder operation in respect to the external low-speed reference clock "cref". Input parallel data "d00-09" initially aligned to the external input low-speed clock "cli" is resynchronized in FIFO by the internal clock "crd". FIFO reset performed by "res" signal, as well as error indicator "err" are incorporated into the design. To increase the flexibility of parallel interfaces "d00-09" and "q00-09", bit order inversion function controlled by "bitordt" and "bitordr" signals is implemented in both MUX and DMUX.

Three internal loop-back test modes are incorporated into the design. In the first mode activated by "lbt1" signal, the parallel data from DMUX outputs and corresponding low-speed clock "cb1" are redirected to MUX inputs through selector SEL1. In this mode, high-speed serial output signal "qhs" should be compared with high-speed input serial signal "dhs" usually provided from a PRBS (pseudo-random binary sequence) generator. In the second mode activated by "lbt2" signal, the high-speed signal from MUX output is looped back to DMUX input through selector SEL2, and parallel CMOS input and output interfaces are used for the control of transponder operation. The third test mode activated by "lbt3" signal is similar to the second test mode but provides a by-pass of CDR. In this mode, the output data

from MUX and corresponding clock “cb3” are delivered to DMUX inputs through selector SEL3.

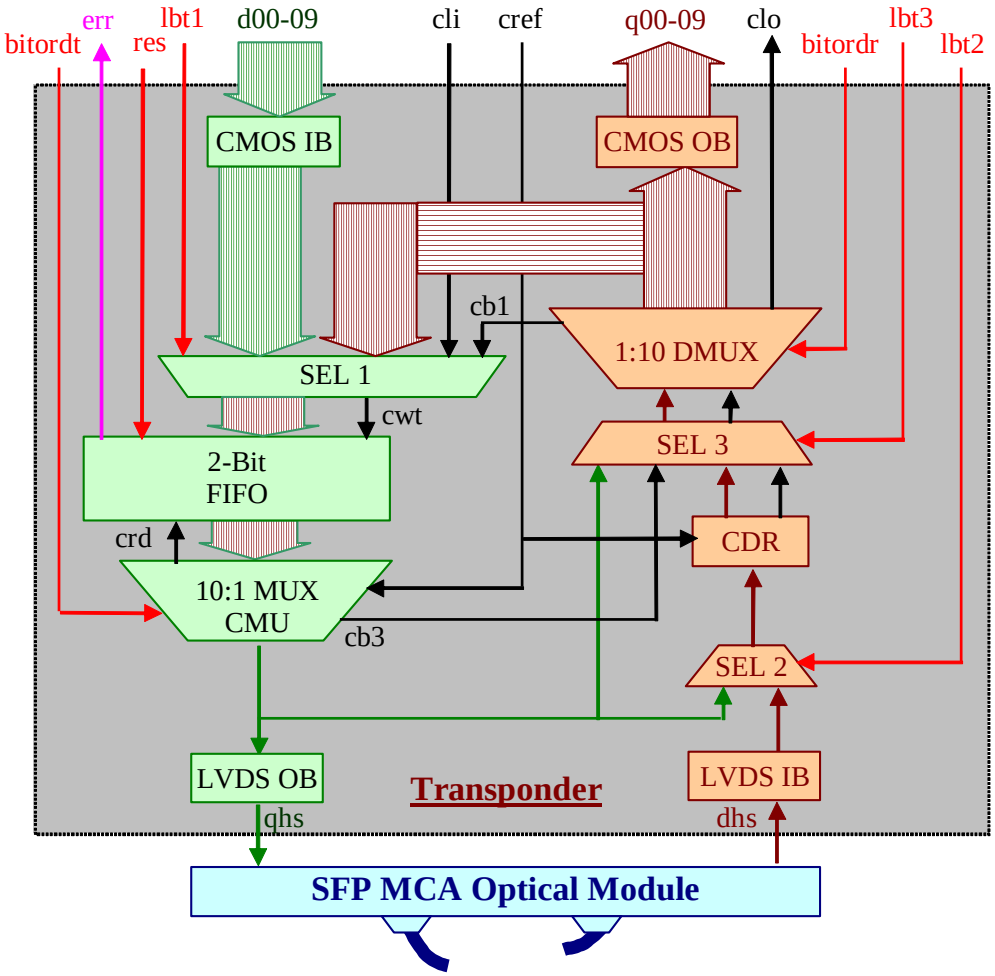

Fig. 1. Transponder Top-Level Block Diagram.

3 Library-Based Design Approach

The complete SERDES is designed within a library of basic cells and functional blocks that has been developed in a 90*nm* CMOS technology. This approach allows for application of previously verified cells and block in new products, which significantly reduces their cost and design time. All cells and blocks in the developed library utilize custom-built transistor structures that provide an improved tolerance to space environmental conditions.

3.1 Library of Basic Cells

CMOS logic is a natural implementation of Si-based CMOS technologies [3]. This single-ended architecture based on FETs with gate lengths of 90*nm* and below is now utilized in most of the modern IC products. At the same time, the short-channel devices suffer from increased sub-threshold currents and low breakdown voltages. They also cannot overcome the natural drawbacks of the single-ended circuitry that includes generation of a switching noise that is increasing with the operational speed, and distortion of the signal’s duty cycle. In addition, uutilization of space-oriented protection techniques usually limits the minimum transistor width and thus negatively affects the operational speed of the corresponding

circuits. It should be noted that the absence of DC power consumption does not help the overall performance of the CMOS circuits due to significant increase of dynamic power consumption at higher speeds. In this particular design, analog blocks represented by two PLLs are very sensitive to any source of noise and require a quieter on-chip environment.

The alternative for CMOS is the differential source-coupled logic (SCL) architecture [5-6]. This logic is based on differential current switches with one or more pairs of switching n-FETs which redistribute a stabilized current generated by a special current source. SCL architecture overcomes the problems of the switching noise and duty cycle distortion at the price of certain DC power consumption. SCL circuits are less sensitive to sub-threshold currents and can potentially achieve higher operational frequency. Unfortunately, the limited transconductance of FETs minimizes the architectural advantages due to the requirements for a higher voltage logic swing (not less than $350mV$) to fully switch the tail current from one branch of the switch to the other. The driving capability of SCL logic gates is also relatively low, thus resulting in increased power consumption. This architecture is suitable for the operational speeds in the range of $10Gb/s$, but its performance degrades rapidly at higher frequencies.

The comparison of two architectures was performed on two sets of frequency dividers-by-10 designed and fabricated in the same $90nm$ technology. The test results summarized in Table 2 show that the power consumption of the CMOS version is close to that of the SCL one at frequencies close to $700MHz$. It can be estimated that the SCL version is more power efficient at speeds above $1GHz$. In addition, the SCL architecture is more suitable for the implementation of complex logic functions as can be seen from the number of gates required for the divider design.

Table 2. Divider Comparison

Parameter	***CMOS Version***	***SCL Version***
Operational frequency	$700MHz$	$720MHz$
Power consumption	$1.2[V]\cdot 0.6[mA]=0.72[mW]$	$1.6[V]\cdot 0.5[mA]=0.8[mW]$
Gate count	61	21

Based on the above considerations, the SCL architecture has been selected for the transponder design. The developed library includes 11 families of cells with different current levels optimized for frequencies from DC to more that $2GHz$: 2-input AND gates, 1-input Buffers with and without input-level compensation diodes, 2-input dual Source Followers – level shifters, D-Latches with and without set/reset functions, 2-to-1 Multiplexers, RS Flip-Flops, Generators of the top logic "0" voltage level $V^{0t}=V_{CC}-\Delta V_L$, 2-input XOR gates, and 2-input SCL-to-CMOS converters.

All cells operate from a $1.8V$ power supply with tail currents generated by two-transistor cascode current sources controlled by temperature-stabilized band-gap reference sources. The achieved voltage accuracy is within ±1.5% over the temperature range of -55°C to 125°C, ±10% variation of supply voltage, and ±3σ variation of technological parameters. An example of the designed cell is shown in Fig. 2. This stabilization allows for the minimization of the internal voltage swing to $350mV$, which improves the speed performance of the circuits. As a result, a cell with a current level of $280\mu A$ can reliably process signals with a frequency up to $1.3GHz$.

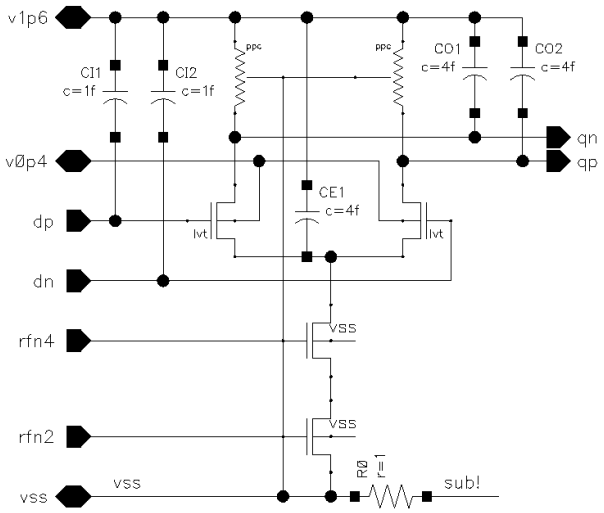

Fig. 2. SCL Buffer.

The library also includes extra low-power 1.3*Gb/s* LVDS output buffers and universal input buffers with increased tolerance to common-mode voltage variation, which are described in [7-8]. The output buffer operates from a 1.6*V* supply voltage generated by an internal voltage source with feedback stabilization.

3.2 Upper-Level Blocks

The most critical parts of the transponder are CDR and CMU. CDR uses the architecture with a phase – frequency detector (PFD), Alexander phase detector (PD), and 2-input charge pump as shown in Fig. 3.

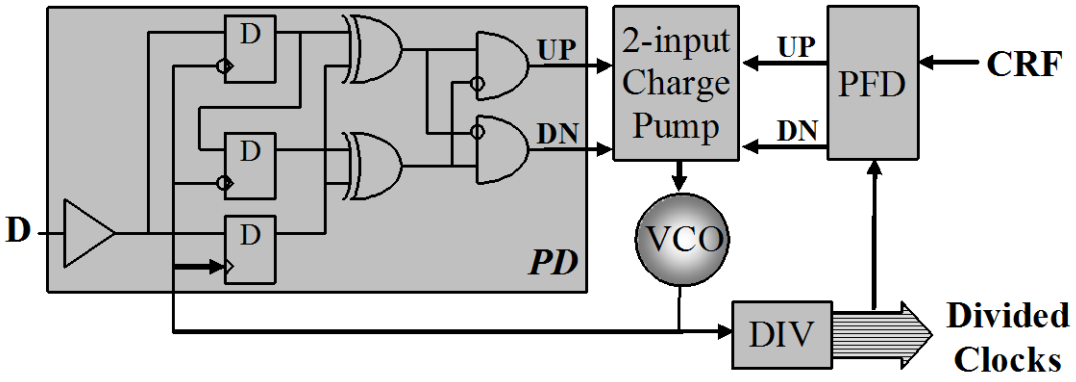

Fig. 3. CDR Architecture.

The 1.25*GHz* voltage-controlled oscillator (VCO) is designed as a ring oscillator with balanced loadings to ensure matching operational modes for all stages of the ring. The tuning range from 950*MHz* to 1.5*GHz* has been achieved with 5-stages of a proprietary voltage-controlled delay cells. The sell is designed as SCL D-type latch with a linearized clock differential pair that operates as the delay control current switch. The schematic of the delay cell is shown in Fig. 4.

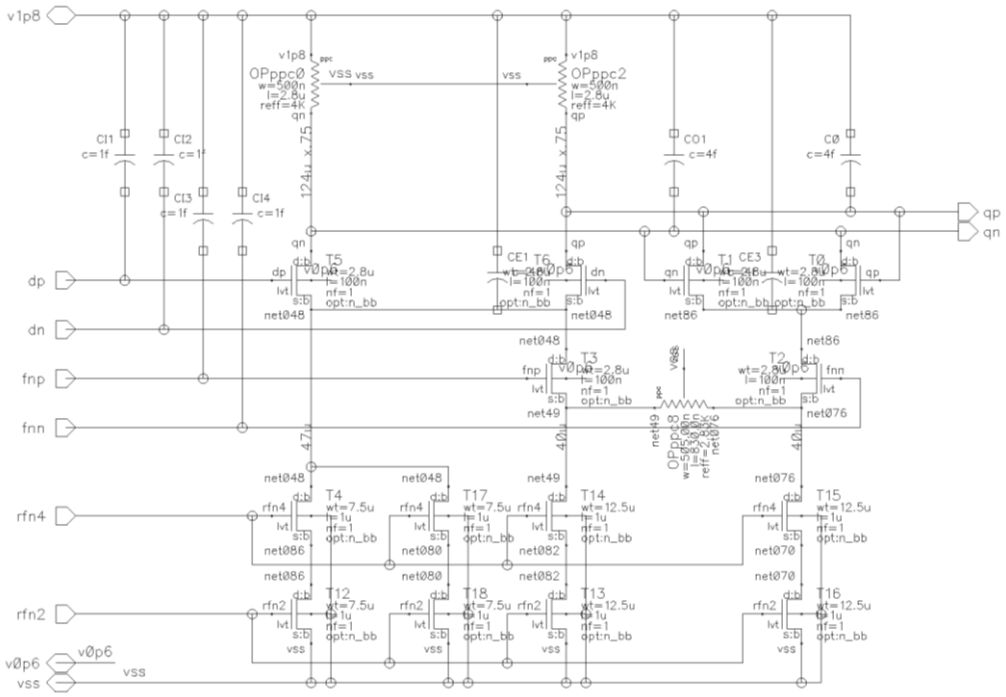

Fig. 4. Voltage-Controlled Delay Cell.

The CMU utilizes similar VCO and PFD blocks but a different 1-input charge pump. All other blocks are designed from standard library cells.

MUX and DMUX utilize a combinational tree-register architecture due to the ratio not equal to a power of 2.

FIFO includes 10 identical blocks for processing 10 bits of data and an error generation block. Each FIFO block writes in a bit of data using the input clock "cwt" and outputs the same bit after its realignment to the output "crd" clock. The initial reset of the block sets the read and write events as far as possible on the time scale and then allows for $\pm(T\text{-}t_{su})$ phase deviation between two clocks. Here T is the clock period and t_{su} is a setup time of internal flip-flops. If the accumulated phase difference exceeds the specified value, the error generator provides a special error signal. This block operates as a phase detector and monitors the phase difference between two clocks. The phase difference equal or less than t_{su} sets the block's output to logic "1" state that indicates the error condition. Assuming slow phase changing rate (temperature or similar conditions), the block is designed to deliver the error signal before any actual errors in the data sampling may occur.

4 CHIP FABRICATION AND TESTING

The complete transponder has been fabricated in a 90*nm* technology. The chip with the dimensions of 2.4x2.4mm^2 has 68 bonding pads, has been packaged into a 68-pin QFN package, and consumes about 80*mA* of current from a single 1.8*V* power supply.

The test board shown in Fig. 5 incorporates the transponder chip, an SFP MSA optical module, SMA connectors for low-speed and high-speed data and clock signals, and control switches. The device was tested in electrical and optical modes and demonstrated the operation in accordance with computer simulations.

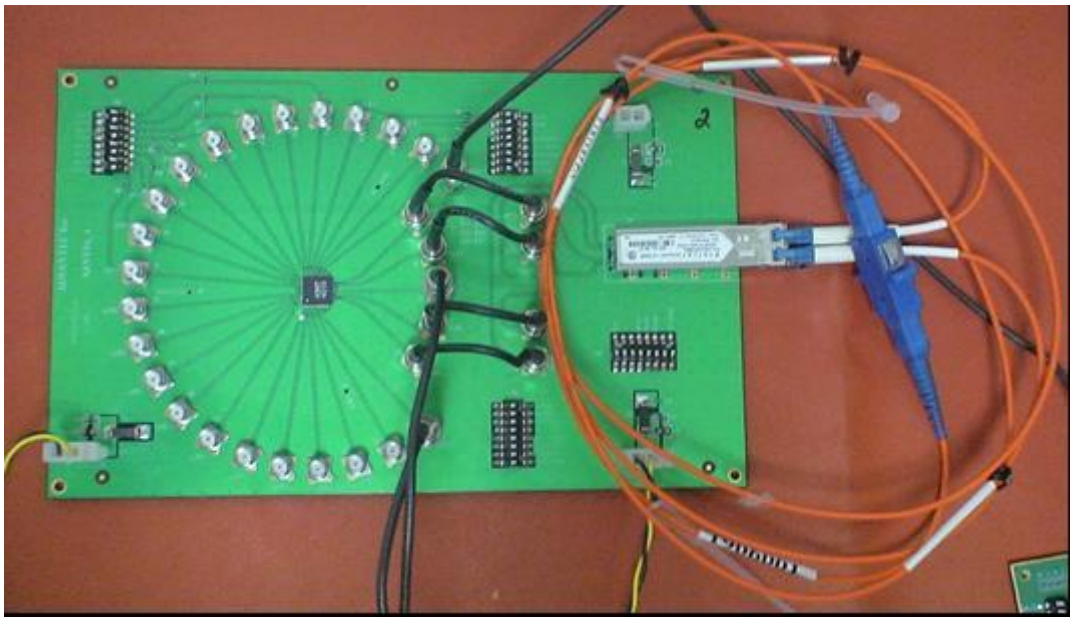

Fig. 5. Transponder Evaluation Board Configured For Optical Testing.

The sample results of the electrical test shown in Fig. 6 demonstrate the output low-speed clock and serial high-speed data with the rate of 1.25*Gb/s*.

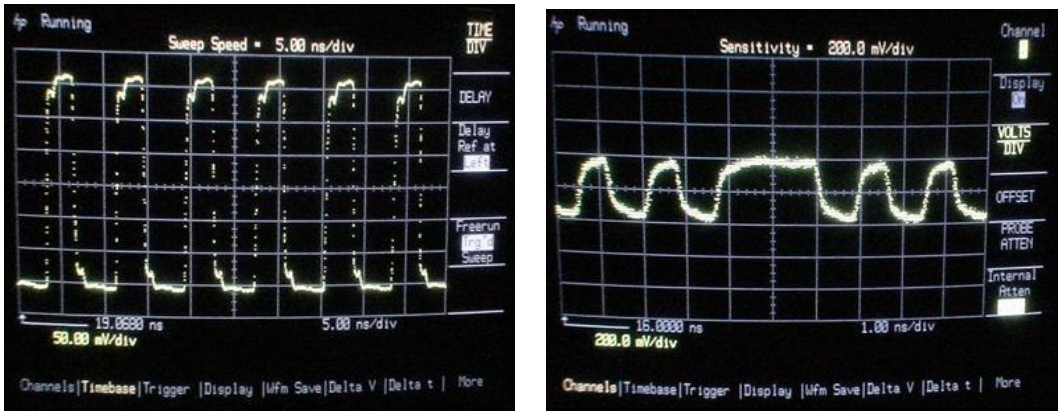

Fig. 6. Output Low-Speed Clock (a) and 1.25Gb/s Output Data (b).

In the optical mode, the output LVDS signal of the Transmitter is converted into light by the optical module and sent through the fiber back to the optical input of the same module. The converted electrical signal is processed by the Receiver and the outputs of the receiver are compared to the Transmitter input signals. This external loop-back test has proved the complete functionality of the designed transponder.

The chip was also tested in the space-imitation environment and demonstrated less that 1% deviation of its parameters from their normal values.

5 CONCLUSIONS

A space-qualified SW-compatible transponder chip designed and fabricated in a 90*nm* technology has demonstrated a full functionality in normal and space-imitation environments including the data rate of 1.25*Gb/s* at less than 150*mW* power consumption. The design is based on a special SCL library of cells and functional blocks utilizing *n*-FETs as active components, which is ready for application to other designs of similar mixed-signal products.

6 REFERENCES

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