

SPACEWIRE BACKPLANE WITH HIGH-SPEED SPACEFIBRE LINK

Session: SpaceWire Components

Short Paper

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ABSTRACT

SpaceWire Backplane is a backplane architecture with SpaceWire interconnects between each board. In ISC2008, we proposed that the space qualified, non-high speed backplane connector evaluated and, if the signal assignment is carefully designed, can be used for high-speed data transmission.[1]. On the basis of this result, we developed the SpaceWire backplane prototype with SpaceWire and SpaceFibre links. This backplane prototype includes a passive backplane board with SpaceFibre links of 3 Gbps or higher. We also developed a sample daughter board for functional evaluation that has both SpaceWire and SpaceFibre interfaces. We present the design and implementation of the SpaceWire backplane as well as an evaluation of the high-speed signal quality of the backplane and daughter board prototyping result that includes the SpaceFibre interface implemented.

1 BACKPLANE TOPOLOGY AND SIGNAL ASSIGNMENT

In the backplane interconnection system, high-speed signals are connected between daughter boards via connectors and a backplane. This reduces the number of harnesses needed and improves the integrity of the signal. SpaceWire backplane is a backplane architecture that uses SpaceWire as an interconnect between boards. While SpaceWire is point-to-point link connection, backplane topology and/or router functionality is important. We decided our backplane is passive without any active components like routes because the backplane needs to be reliable and durable. Although there are

various network topologies such as tree, ring and mesh. we selected a backplane configuration as the full mesh topology for the followings reasons.

1. The backplane has to have enough flexibility. While other topologies are a subset of the full mesh topology, the actual configuration can be defined by each satellite and/or purpose of each component.
2. Usually full mesh topology needs too many interfaces to construct a network system. However, almost all components of a spacecraft can be constructed with no more than 8 boards. Therefore backplane needs to have only 7 SpaceWire ports.
3. Full mesh topology can be partitioned in any subset. This nature is useful to make a component redundant. We defined two partitions of 4 slots to our backplane and defined the power supply board connector and control signals to each partition. If full of 8 slots required for 1 component, redundancy can be provided by using 2 chassis connected to each other via external SpaceWire signals.
4. Daughter boards can be independent of slot position if SpaceWire ports are assigned in cyclic symmetrically. The daughter board thus needs to implement only the required SpaceWire ports. For example, for a backplane partitioned in two 4 slots, each daughter board need only the first three SpaceWire ports.

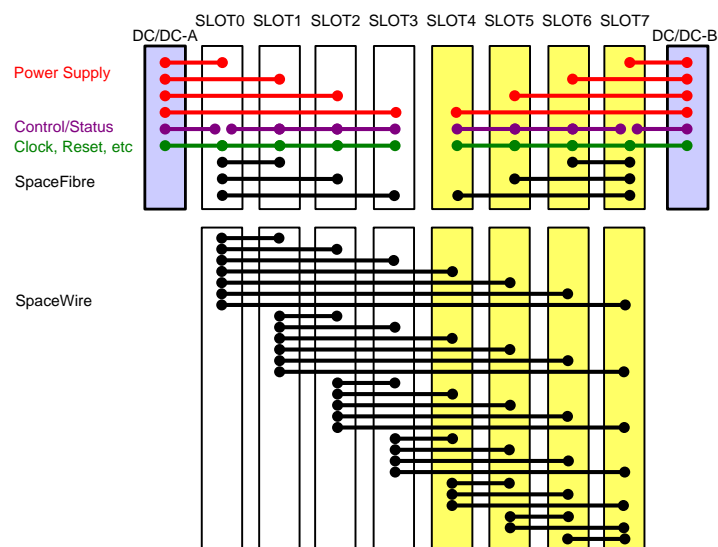


Figure 1 : SpaceWire Backplane topology

On the contrary, we defined Tree topology for SpaceFibre channels because fewer SpaceFibre channels can be assigned to one connector with high-speed signal quality. We suppose the purpose of SpaceFibre channel is for high speed/large capacity data recorder and/or high-speed signal processing boards, so the tree topology is suitable for this purpose. The backplane topology we defined is shown in Figure 1.

The definition of control/status signals is also important as it defines the topology of the SpaceWire topology. We defined clock, timing pulse distribution, power control/status, slot ID and reset signals. We also defined slot0 and slot7 as control master slot of other slots. The control master slot controls power on and off via power control/status signals.

We also defined mechanical design including chases and daughter board. As the mechanical design is based on our existing components, using this prototype to develop the flight model is rather easy. The daughter board is designed with upper compatibility to a 6U Euro card. The circuits designed for this card are easily implemented onto the daughter board because the circuit-populated area excluding frame structure is same as that of the 6U Euro card. The prototype specification is shown in Table 1.

Number of slots	8 + 2(DC/DC)
Number of channel	SpaceWire : 7ch for each slot
	SpaceFibre : 3ch for slot0 and slot7, 1ch for other slots
Topology	Full mesh(SpaceWire), Tree(SpaceFibre)
Dimensions	Chassis : 290 mm x 253 mm x 264 mm
	Daughter board : 265 mm x 223 mm
Backplane connector	110 pins x 2 / slots

Table 1 : Prototype backplane and chassis specifications

We developed and evaluated SpaceWire backplane prototype. While we presented 3Gbps signal integrity in ISC2008[1], we designed this prototype to transmit signals up to 6.25Gbps because SpaceFibre maximum transfer rate target is 6Gbps. To achieve this high-speed signal capability, we also designed an equalizer for high-speed signal lines. The daughter board with the SpaceWire and SpaceFibre interfaces is also developed to validate functionality of the backplane system. In addition to the SpaceWire codec we have already developed[2], SpaceFibre codec is developed to this daughter board. A block diagram of the daughter board we developed is Figure 2. In addition to backplane connector signals, two SpaceWire and two SpaceFibre connectors are assigned in front. All SpaceWire and SpaceFibre codec channels, and a small processor for debug and port control and switch fabric are integrated into FPGA. The first implementation of SpaceFibre codec works in loopback mode. We are planning an interoperability test with other SpaceFibre implementations to validate and improve the SpaceFibre specification.

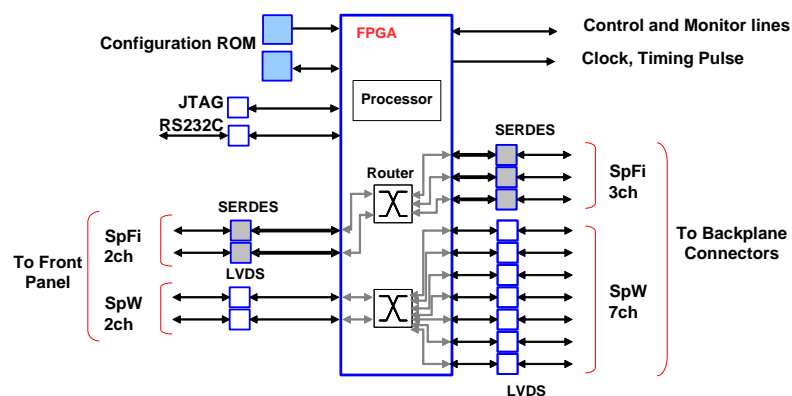


Figure 2 : Daughter board block diagram

The backplane board, the daughter board and the chassis we developed are shown in Figure 3 and the measurement of transmission characteristics and eye pattern of 6.25Gbps backplane signal are shown in Figure 4. Our equalizer significantly

improves both transmission characteristics and eye pattern. This result shows our backplane design transmits data at 6.25 Gbps.



Figure 3 : SpaceWire backplane (left), daughter board (center), and chassis (right)

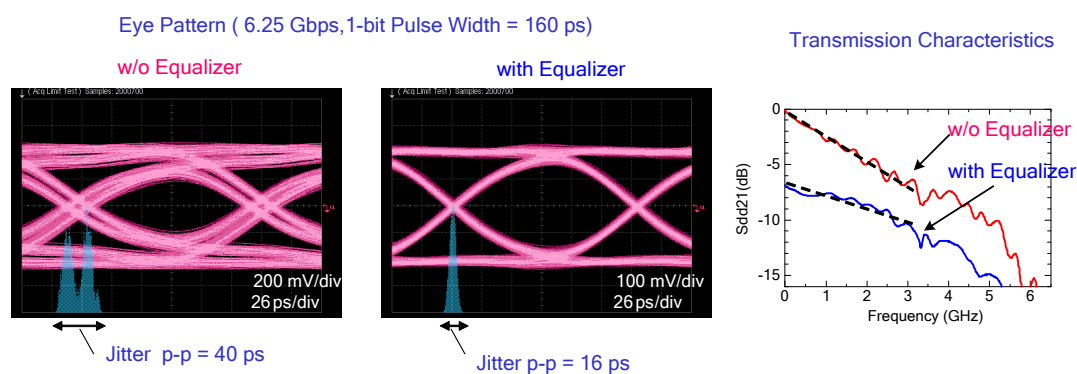


Figure 4 : Evaluation of high-speed signal transmission

2 CONCLUSION

We defined SpaceWire backplane architecture including network topology, signal assignment, and mechanical design. We then developed the prototype of backplane and daughter board with a chassis to evaluate our backplane system. The evaluation result of the backplane signal integrity is enough to transmit a 6 Gbps high-speed signal via a space-qualified connector. We also implemented SpaceFibre codec for our daughter board. The first implementation works with a loopback test and we are planning to test interoperability with other implementations.

3 REFERENCES

1. Shibuya, Yamagishi, Oh-hashii, Saito, Nomachi, "Evaluation and Analysis of Connector Performance for the SpaceWire Back Plane", International SpaceWire Conference 2008, Nov.2008, pp 83-86.
2. Sasaki, Nakamura, Yoshimoto, Yoshida, Yoshikawa, "A CPU Module for a Spacecraft Controller with High Throughput SpaceWire Interface", International Conference SpaceWire Conference 2008, Nov.2008, pp 181-184