RACE CONDITION FREE SPACEWIRE DECODER FOR FPGA

Session: SpaceWire Components

Short Paper

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ABSTRACT

Data-Strobe encoding is a simple encoding system. A clock signal is simply recovered by the exclusive OR of Data and Strobe. However, this simple decoder causes race condition. When Data line changes the logic level, the recovered clock also changes the logic level. Therefore, the recovered clock and the Data are in race condition. Race condition obstructs portability of the decoder logic in FPGA.

We have developed the DS decoder to avoid race condition, which works up to the maximum speed of FPGAs. The race condition free decoder is portable to any FPGAs.

1 INTRODUCTION

Data-Strobe encoding is easy to be decoded with small amount of logic in a FPGA. Recovered clock by the exclusive OR of Data signal and Strobe signal can be used for decoder logic (Figure 1). However, this simple way causes race condition. Data signal and recovered clock may change at the same moment (Figure 2). Therefore, the recovered clock and the Data signal are in race condition. The behaviour of this simple logic depends on propagation delay and set-up/hold time of the FPGA. They depend on the

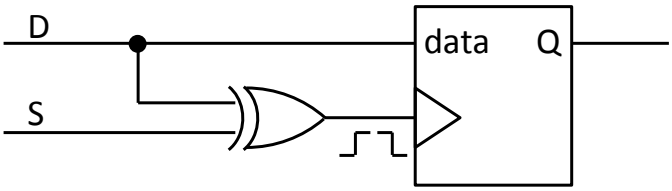

Figure 1: DS decoder logic

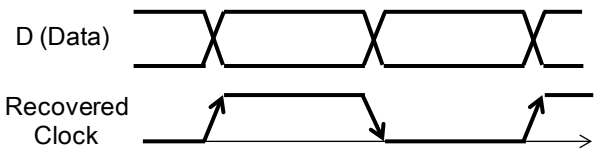

Figure 2: Wave form of Data signal and recovered clock.

routing in the FPGA chip. Thus, race condition obstructs portability of the decoder logic in FPGA. It should be noted that race condition stay also in slower bit rate.

Simple solution to avoid race condition is to synchronize the input signals. It is safe and simple way. However, the sampling interval must be shorter than the bit duration. Therefore, this kind of decoder cannot extract maximum performance of the FPGA compare to the simple decoder logic which uses the recovered clock. In this paper, we present new idea to avoid race condition, which works up to the maximum performance of FPGAs.

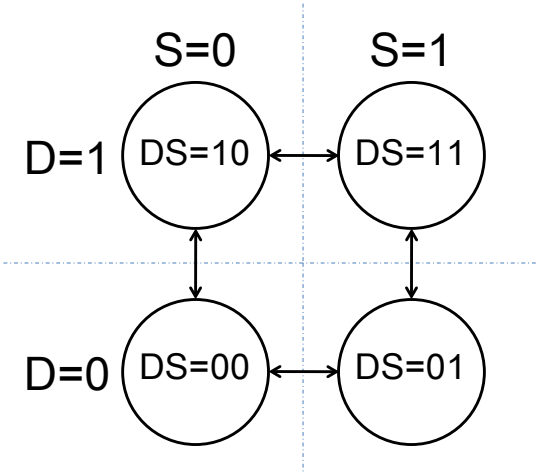

Figure 3: State diagram of Data (D) and Strobe (S).

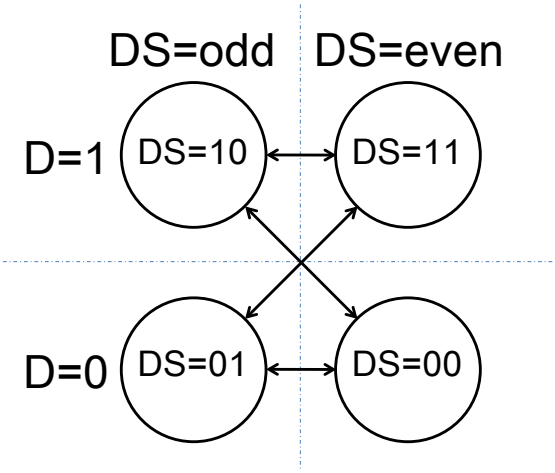

Figure 4: State diagram of D-S signals.

2 STATE DIAGRAM OF INPUT SIGNALS

We examine the behaviour of D (Data) and S (Strobe) in DS encoding. The figure 3 is a state diagram of D and S. There are no transitions between orthogonal states, which are caused by simultaneous change in both D and S. In DS encoding, simultaneous change of D and S does not happen.

The figure 4 also shows the state diagram but lower two states are twisted. States are classified by “parity” of “DS”. DS odd state is DS=”10” or DS=”01”. DS even state is DS=”11” or DS=”00”. In other words, exclusive OR of D and S is “1” in DS odd states and “0” in DS even states. DS odd states and DS even states appear alternatively (Figure 5).

The appearance rate of even/odd states is half of the bit rate. DS even state starts at the falling edge of the recovered clock. DS odd state starts at the rising edge of the recovered clock. Therefore it is possible to extend those states until the next occurrence, which is at the two bit after.

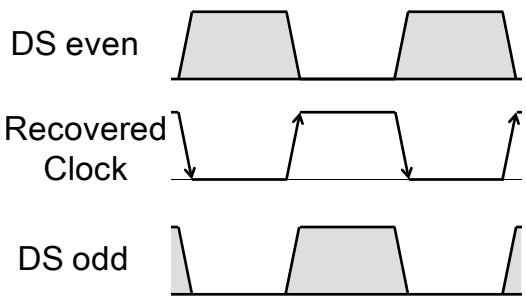

Figure 5: Wave form of DS even state and odd states

3 RACE CONDITION FREE LOGIC

Dividing the input states into two groups (even and odd), the frequency of the state in each group is a half of the bit rate (Figure 6). Extended even state changes the state at the falling edge of the recovered clock but does not change the state at the rising edge. Therefore, extended even state and the rising edge of the recovered clock are not at race condition. Extended odd state changes the state at the rising edge of the recovered clock but does not change the state at the falling edge. Therefore, extended odd state and the falling edge of the recovered clock are not at race condition.

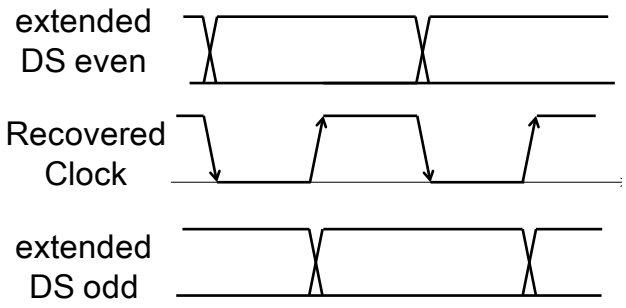

Figure 6: State diagram of D-S signals.

We split the state in to two groups, which are DS even states and DS odd states. The state is extended using asynchronous set / reset (Figure 7). The even/odd state is held for two bit duration.

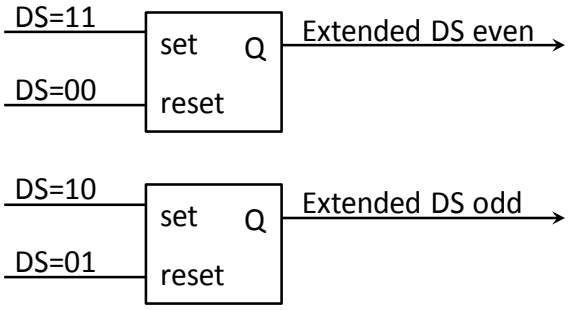

Figure 7: Extended even/odd state

Race condition free decoder logic is shown in the figure 8. Since the extended even/odd states are held for the duration of two bits, the logic of this stage works at higher bit rate compare to the simple decoder logic. However, merging even states and odd states to obtain the "character", only one bit duration is allowed. Consequently, maximum bit rate is the same as the simple decoder logic but not less.

4 SUMMARY

Because of race condition, the simple DS decoder logic is not portable. In order to avoid race condition, input states are divided into two groups using DS parity. Even parity state and odd parity state appear alternatively. They can be handled without race condition. This race condition free decoder logic works at maximum speed of implemented FPGA.

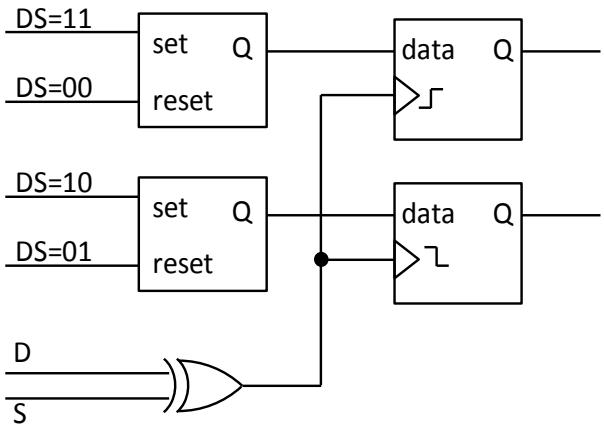

Figure 8: Race condition free decoder logic