ASTRIUM'S SPACEWIRE BASED LEON PROCESSORS

Session: SpaceWire Components

Short Paper

Paul Rastetter, Tim Helfers, Mark Hartrampf

Astrium GmbH, 81663 Munich, Germany

Jean-Luc Poupat

Astrium SAS, 78997 Elancourt, France
E-mail: paul.rastetter@astrium.eads.net, tim.helfers@astrium.eads.net, mark.hartrampf@astrium.eads.net, jean-luc.poupat@astrium.eads.net

ABSTRACT

There are two SpaceWire based processors in Astrium. One is named SCOC3 and one is named MDPA. SCOC3 uses LEON3-FT and MDPA uses LEON2-FT, both processors are based on SPARC V8 standard.
The main application of SCOC3 is platform while MDPA's main application is payload. The paper describes the different interface modules used to achieve the functionality and also the commercialisation aspects of the two processors.
MDPA (Multi-DSP/micro-Processor Architecture) is a highly integrated System-on-Chip system, which is an advancement on the architecture developed and used on the Inmarsat4 DSP payload. The MDPA is a concept based on a matrix of data processing nodes interconnected using SpaceWire (SpW), with external SpW interfaces to enable connection to other telecommunication, earth observation or science payload subsystem. An MDPA node is in effect a system-on chip which incorporates a highly integrated DVB-S modem co-processor combined with a powerful LEON2-FT microprocessor function and relevant interfaces all integrated on the same device. This architecture acts as the controlling unit for the Data Path Subsystem (DPS) within the frame of the next generation of digital telecommunication payloads. Additionally the MDPA concept is laid out for high end control applications or medium rate data processing for earth observation or science payloads.
The 8 SpaceWire interfaces can be used to interconnect several MDPA nodes to a multi-processor configuration. This increases the overall processing performance and enhances the processing redundancy since a faulty node can be replaced by another one. The routing capabilities support the communication of the nodes with low processor interaction. In addition the high number of SpaceWire interfaces allows connection of several remote controlled devices for command and monitoring of subsystems.
The modem function is implemented as hardwired block on-chip. Other devices such as GNSS receivers or reconfigurable co-processors can be used externally and controlled via SpaceWire.

SCOC3 is based on 7 independent AMBA controllers programmed individually by the SPARC processor. They work by using DMA mechanisms to access a specific memory and to free the processor. They are allocated to CCSDS communications, I/O User communication, Reconfiguration of satellite's system and tests links.
All these SpaceWire links are compliant to the last ECSS standard and are RMAP compatible.

MDPA Technical Overview

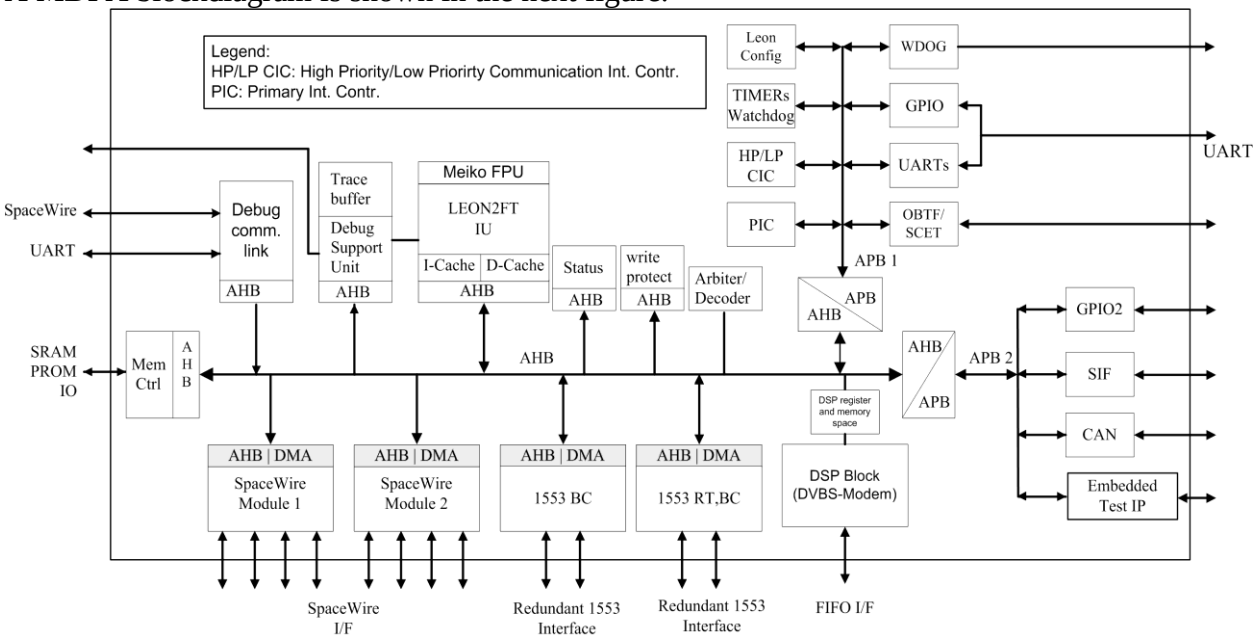
MDPA is a highly integrated System-on-Chip system. This architecture offers the benefits of efficiency and the savings provided by a hardwired DSP and the flexibility offered by a programmable microprocessor system, joint together using state-of-the-art interconnection IP.
The main tasks of MDPA are

- (de-)modulation and (de-)coding capabilities for regeneration of telecommand and generation of telemetry channels
- Supervise, configure and monitor the Data Path Subsystem (DPS)
- Interface with spacecraft central computer

The functionality is provided by means of the following functions, integrated into a single chip.

- The fault tolerant microprocessor core LEON2-FT
- A digital signal processing module
- Various interfaces (SpaceWire with routing capabilities, MilBus, CAN bus)

A MDPA blockdiagram is shown in the next figure.



MDPA Processor core

The processor core is based around the LEON2-FT using one AMBA AHB bus and two APB buses. The APB buses are connected via bridges to the AHB. The following main communication interfaces are provided

- 8 SpaceWire links
- 2 redundant MILBUS
- 1 CAN bus

One set of SpaceWire interfaces are used to interconnect several MDPA nodes to a multi-processor configuration. This increases the overall processing performance and enhances the Fault Detection, Isolation and Recovery (FDIR) capabilities since a faulty node can be replaced by another one. The other SpaceWire interfaces are routed to the Data Path Subsystem carrying the switches and beamformer configuration data.
The MDPA contains a CAN bus interface for low data rate data transfers to nodes and peripherals. The Service Interface (test interface) based on SpaceWire is used for advanced software debugging support as memory load commands etc. with 100 Mbps data rate.

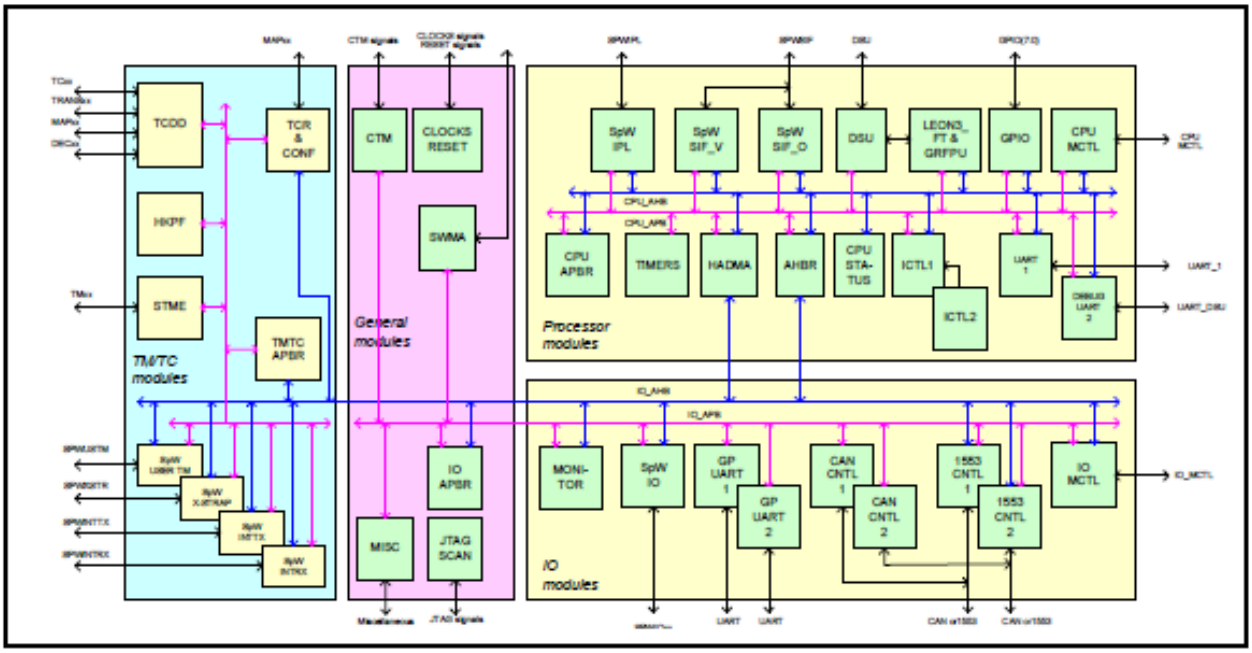
MDPA DSP module

The DSP module is equipped on each MDPA node and demodulates and decodes the incoming time-division multiplex (TDM) telecommands coming from the Network Control Center. Additionally the data dedicated for downlink telemetry are coded and modulated.

SCOC3 Technical Overview

The Satellites are controlled via a platform computer that permits the control of the satellite (attitude, orbit, modes, temperatures …) with respect to its payload mission (communication, earth observation, scientific mission). The platform computer is connected to the satellite and the ground control via digital links and executes onboard software. On a hardware point of view, it gathers a lot of digital functions, usually dispatched on numerous devices, in a single device.

At architectural level there are two memory interfaces, one dedicated for the LEON3-FT and another one for the peripheral IOs (SpaceWire, 1553 mil-bus, TM/TC) and an AMBA architecture/DMA for the performance.



A SCOC3 blockdiagram is shown in the next figure.

SCOC3 Processor core

SCOC3 is based on LEON3-FT. There are two AMBA AHB buses, one dedicated to the processor and one to interfaces functions. Both are linked by a bridge. They are used to transfer data. There is an APB bus for configuration of functions. APB and AHB are linked by a bridge.

The following main communication interfaces are provided

- 7 SpaceWire links
- 2 redundant MILBUS
- 2 CAN bus

The 7 SpaceWire links are allocated to different functions. Two are allocated to TM/TC, two for cross-strapping and the others are user's free.

The implemented CCSDS TM/TC functions are dedicated to satellite/ground communications through the satellite transponder. These functions work either with the processor or in stand alone. There is a specific CCSDS TM/TC area dedicated to communication between the satellite and the ground through the satellite transponder.

Technology and Packaging

MDPA and SCOC3 are realised as ASICs in Atmel's space qualified 180 nm technology, called ATC18RHA. MDPA is delivered in a CQFP 352 pin package and SCOC3 in a 472 pin Column Grid Array package (CGA).