NEXT GENERATION DSP MULTI-CORE PROCESSOR WITH SPACEWIRE LINKS AS THE DEVELOPMENT OF THE "MCFlight" CHIPSET FOR THE ON-BOARD PAYLOAD DATA PROCESSING APPLICATIONS

SESSION: SPACEWIRE COMPONENTS

Short Paper

Tatiana Solokhina, Jaroslav Petrichkovich, Alexander Glushkov, Yury Alexandrov, Andrew Belyaev, Ilia Alekseev / *ELVEES R&D Center of Microelectronics, Moscow*, Yuriy Sheynin */ St.Petersburg University of Aerospace Instrumentation*

E-mail: secretary@elvees.com, sheynin@aanet.ru

ABSTRACT

The paper presents the architecture of the high performance prospective processing SoC with communication protocol SpaceWire as the Next Generation DSP Multi-core Processor for Onboard Payload Data Processing Applications.

1 INTRODUCTION

The DSP Multicore processor continues processors road map which begins from dual cores processor 0.25-um MC-24R (from the "MCFLIGHT" chipset) for signal processing and control distributed architectures with SpaceWire interconnections that is produced by the "ELVEES" company (Moscow). The structure of the chip (Fig. 1), includes the following main components:

- CPU - central processing unit based on the RISC-core and floating-point IEEE 754 standard coprocessor (FPU);
- DSP - multicore unit (from 4 up to 8 cores) for digital signal processing;
- XRAM, YRAM - the DSP memory;
- CRAM - CPU RAM;
- CDB - CPU data bus;
- MPORT - external memory port;
- DDR_PORT0, DDR_PORT1 - ports of the DDR memory;
- DMA -direct memory access controller;
- OnCD - built-in unit for the programs debugging;
- UART - Asynchronous serial port; USB Controller; I2C controller;
- AXI Switch;
- PLL - frequency multiplier based on PLL;
- Ethernet 10/100 MAC-controller;
- SWIC0, SWIC1 – standard Space Wire serial links controllers;
- GigaSWIC0, GigaSWIC1 - Giga SpaceWire serial links controllers;
- PMSC - PCI bus controller;
- VPIN - video input port; VPOUT - video output port;
- MFBSP® (Multi Functional Buffered Serial Port) – ELVEES s patented multi buffered serial port (SPI, I2S, LPORT, GPIO);
- ICTR - interrupt controller;

– IT - interval timer; WDT - watchdog Timer; RTT - real-time Clock;
– JTAG - debugging port.

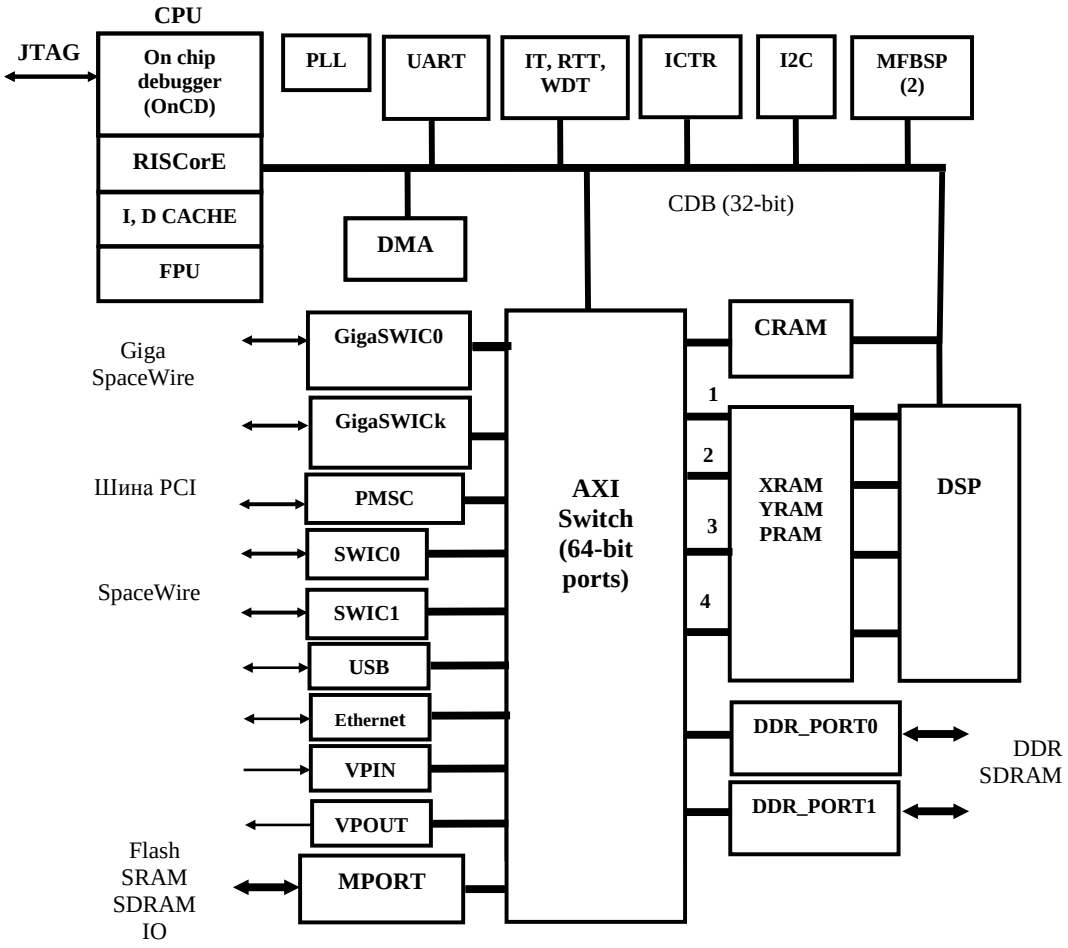

Fig. 1 Block diagram of the Multicore signal microprocessor.

Multicore signal microprocessors include the high-performance IP-cores (RISC-based CPU and DSP), embedded SpaceWire links and high throughput gigabits links, such, as sRIO, GigaSWIC® or and SpaceFibre. CPU core can be used on the base of any processor platform with an interface AXI (for example, RISCore32 (MIPS32 architecture CPU) of the MULTICORE IP-platform libraries).

As the DSP the new ELVEES 'DSP-configurations clusters from ELVEES' MULTICORE IP-core library can be used: QELcore-09™ DSP-cluster or OCTEL-core-09™ DSP-cluster. They contain 4 or 8 programmable cores (Fig.2 and Fig.3) with fixed and floating point (ELcore-™ DSP-core family, Tabl.1).

All processors in the chip operate independently of each other (each with its own program) and, therefore, represent a system-on-chip MIMD - architecture (MIMD - Multiple Instructions Multiple Data).

The most important devices in the structure of the processor are intelligent direct memory access (DMA) engines, which can provide mutual synchronizations, for example, GigaSWIC with DSP-cores.

In this case are possible both options of the MIMD-organization:

(A) CPU carries out the function of the general manager of the Executive programs, directs the DSP-cores and DMA devices, and the DSP-core is an intelligent accelerator operating on its own the program and having the

opportunity of independently initialization to implement its software. CPU has access to all processors resources.

(B) CPU and DSP - cores both have access to the chip resources. DSP have access to the entire address space of the chip, including registers, DMA-channels and peripheral blocks. With simultaneous access to the same resources the priority is given to the CPU.

2 DSP FEATURES

ELVEES DSP-cores main features:

- two 128-bit data memory accesses (X & Y) each cycle;
- vector operations, scalable 1/8/16/32/64/128 bit data formats;
- VLIW-type instruction set;
- Fixed-point and floating-point (IEEE-754) operations;
- Short (up to 7 phases) pipeline;
- AMBA AXI external bus interface;
- Non-Uniform Memory Access.

Tabl.1 ELcore-xx™ DSP-core family

DSP- core	Pipeline	SISD/ SIMD	Program memory	Data memory	Process, nm	Clock, MHz	Perform-ance, MFLOPs	Silicon proved
ELcore-14 ™	3	1	4Kx32	36Kx32	250	80	240	+
ELcore-24 ™	3	2	4Kx32	40Kx32	250	80	480	+
ELcore-26 ™	4	2	4Kx32	16Kx32	250	100	600	+
ELcore-28 ™	7	1	8Kx32	32Kx32	180	250	1500	+
ELcore-30 ™	7	1	8Kx32	32Kx32	130	300	1800	+
ELcore-09 ™	7	1	8Kx32	32Kx32	90	500	3000	-

ELVEES' DSP- cluster main features:

–AMBA AXI external bus interface;
–Non-Uniform Memory Access Architecture;
–"Floating boundary" of the data and program memory.

Tabl.2 ELcore-xx™ DSP-cluster family

DSP- cluster	DSP- core	Num-ber of cores	Program memory	Data memory (NUMA)	Process, nm	Clock, MHz	Perform-ance, MFLOPs
QELcore-28 ™	ELcore-28 ™	4	4x 8Kx32	128Kx32	180	250	6000
DELcore-30 ™	ELcore-30 ™	2	2x 8Kx32	64Kx32	130	300	3600
QELcore-09 ™	ELcore-09 ™	4	4x 8Kx32	128Kx32	90	500	12000
OCTELcore-09 ™	ELcore-09 ™	8	8x 8Kx32	256Kx32	90	500	24000

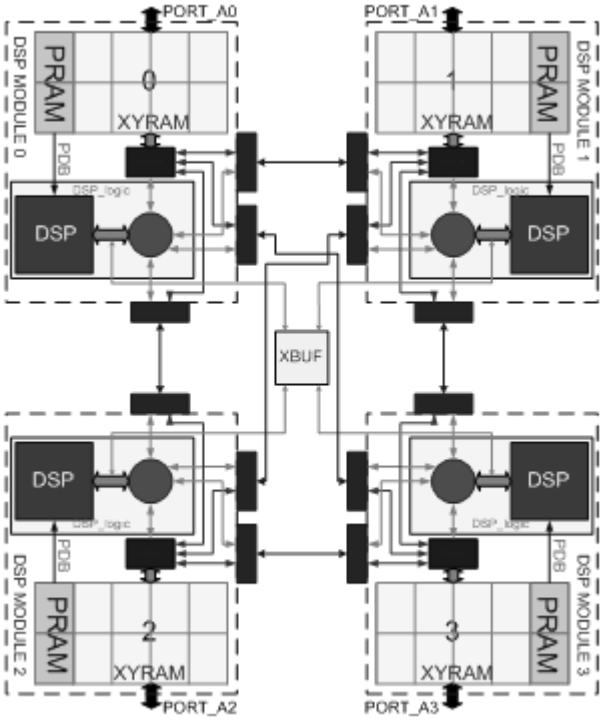

Fig.2. QELcore-09 ™ DSP-cluster block diagram

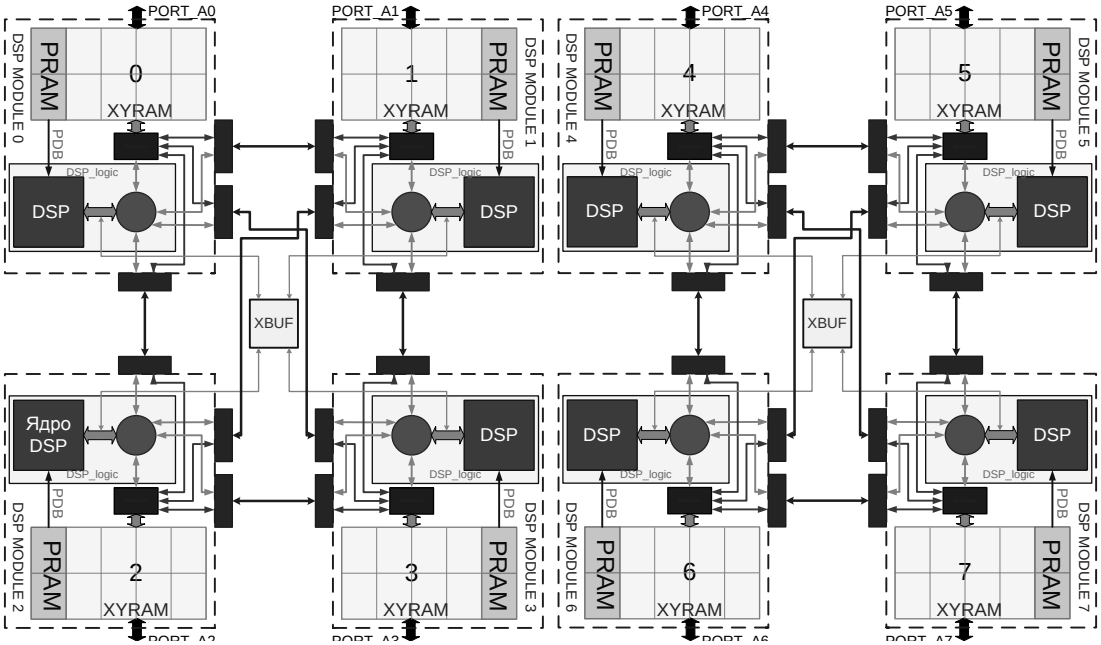

Fig.3. OCTELcore-09 ™ DSP-cluster block diagram

DSP provides the Gflops or Bops level of the performance. For example, 200 operations in 16b format or 48 floating point (IEEE754, single format) operations are performed at the same time at one clock in the OCTELcore-09™ DSP-cluster.

Therefore, necessary conditions for balancing of such a high DSP performance and data flows speed are:

A) Presence of a large number of DMA on chip devices operating with DSP;

B) Rapid channel exchanges with external devices - Giga SpaceWire serial links (GigaSWIC™).

3 GIGA SPACEWIRE SERIAL LINKS

It is important to implement the high-performance – high-rate and low latency, data transfer with low overheads and low power and area implementation costs. General purpose high-rate interconnections – Serial RapidIO, Infiniband, FibreChannel don't fit this set of requirements. The SpaceWire technology has better characteristics, though its data rate could be not enough to support the DSP-clusters performance even with parallel processing logic clustering. Higher data rates are promised by SpaceFibre (in development). Another way here could be SpaceWire evolution to Gigabit link rates. While forcing the existing SpaceWire link rates from 0,4 Gb/s in the standard (up to 0,6 – 0,8 Gb/s in some Russian and US implementations), with modification of the SpaceWire protocols low levels only, the rates of 2,5 – 5 Gb/s could be achieved in used for Multicore technologies. It uses 8b/10b coding and recoding of characters at the Symbol level. We call this modification Giga-SpaceWire, its controller core - GigaSWIC. We don't see reasonable to implement byte-level multilane links; packet level inverse multiplexing over multiple links looks more flexible and better in cost/performance space.

Along with SpaceFibre technology development finalising correspondent SpaceFibre link controller will be designed and incorporated into Multicore DSP chips along with, or instead of, the GigaSWIC cores.

The developed Multi Core DSP and scalable number (2-4) of SpaceWire/GigaSpaceWire/SpaceFibre links integrated on a System on Chip will enable the high performance on-board processing required for future missions. Integration of Multicore DSP chips into scalable multiprocessor systems is supported by direct DSP chips interconnection by SpaceWire/GigaSpaceWire links as well as routing switch chips for larger configurations with many DSP SoCs.

DSP Multi-core processor SpaceWire links are supported by drivers in Linux that run on the prototype chips.

4 CONCLUSION

The current project status: RTL code of the Next Generation DSP Multi-core Processor for Onboard Payload Data Processing Applications with GigaSWIC links, 130nm engineering samples and 180nm 5-cores DSP Multi-core Processor with SpaceWire links. The planned technology for SOC is 65 – 90 nm RAD HARD CMOS or SOI that will provide high efficiency (up to tens GFLOPs). The design and architecture must support Single – Event – Upset (SEU) fault-tolerance.

Examples of distributed computer systems Multi-Ray Satellite Relay, Earth Monitoring with small Satellite Radar onboard radar images synthesis & compression, Codec for Multi – Media Standard H264/AVC and JPEG-2000 Image compression, Coder (Convolutional, Reed-Solomon) and Decoder (Viterbi, Turbo), which are based on the "MCFLIGHT" chips, illustrate scalable reference structures for distributed signal processing and real-time control systems with SpaceWire interconnections.