

# SPACEWIRE APPLICATION FOR THE X-RAY CCD CAMERA ONBOARD THE ASTRO-H SATELLITE-THE BBM DEVELOPMENT AND THE EM DESIGN

## Session: SpaceWire Missions and Applications

### Short Paper

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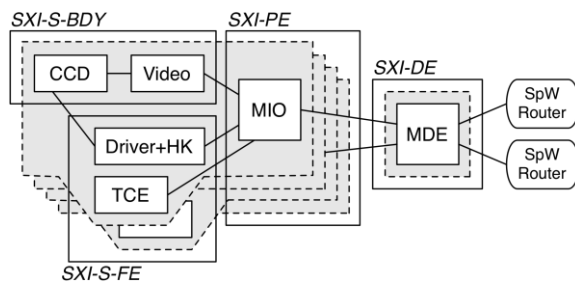
## ABSTRACT

We are developing Soft X-ray Imager (SXI), an X-ray charge-coupled device (CCD) camera system on board the ASTRO-H mission. It has a SpaceWire (SpW) interface and will be installed in the satellite's SpW network. In this paper, we report the results of the breadboard model development and present the engineering model design and architecture under consideration.

## 1 INTRODUCTION

ASTRO-H, Japan's 6th X-ray astronomical satellite, is planned for launch in FY2013. It employs SpaceWire (SpW)-based information network system. And the onboard equipment communicates through the SpW network. The Soft X-ray Imager (SXI), an X-ray charge-coupled device (CCD) camera system in conjunction with the X-ray telescope, is one of the observation instruments. Therefore, the SXI also have to be designed on the assumption that it will be installed in the satellite's SpW network. Since the SpW-based X-ray CCD camera system is a new item we develop, the breadboard model (BBM) has been developed first, and the engineering model (EM) design is currently designed.

## 2 SXI DIGITAL ELECTRONICS

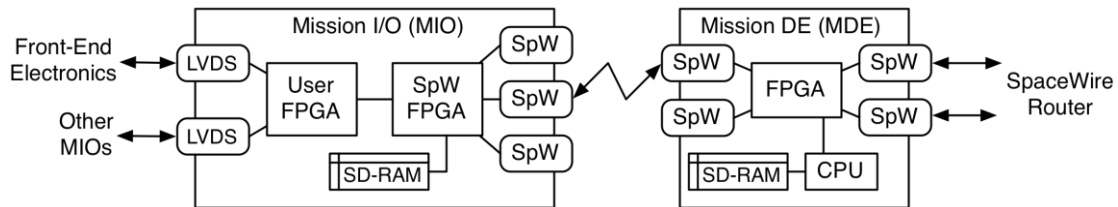


**Figure 1: Schematic block diagram of SXI electronics, which consists of four identical circuits and a CPU unit.**

via SpW network. By RMAP commands from the SXI-DE, the SXI-PE controls peripheral devices, processes CCD pixel data, and collects HK information. The SXI-DE also handles advanced data processing such as an X-ray event extraction.

Figure 1 shows the component diagram of the SXI electronics. Four X-ray CCD chips are in the focal plane, and each CCD chip has the identical driving and readout circuits. The digital electronics is divided into two processing units, an FPGA-based unit (SXI-PE; Pixel-processing Electronics) and a CPU-based unit (SXI-DE; Digital Electronics). Both of them have SpW I/Fs and communicate with each other

### 2.1 THE HARDWARE



**Figure 2: Schematic block diagram of the MIO board and the MDE board.**

The hardware devices for the SXI-PE and the SXI-DE are a Mission I/O (MIO) board and a Mission DE (MDE) board, respectively. “Mission” means that these devices have been developed as BUS equipment in the ASTRO-H mission. That enables us to reduce the costs, speed up the development time, and improve the reliability. Figure 2 shows a schematic block diagram of the MIO and MDE boards. The MIO consists of “User FPGA” in which implemented user logic to serve the purpose of each instrument and “SpW FPGA” that has SpW interfaces. Instrument-specific programs and common SpW interfaces are also installed in the MDE.

### 2.2 THE BBM DEVELOPMENT

We have manufactured the breadboard model (BBM) of the SpW-based CCD camera system, whose DAQ structure is described in Fujinaga et al. 2010 (this conference) in detail. While the BBM hardware is slightly different from those of we show in Figure 2, the basic configuration and functional allocation are similar. We have developed minimum required functions to obtain CCD raw image and implemented them in the BBM system. The BBM works well in the lab system.

## 3 THE ENGINEERING MODEL DESIGN

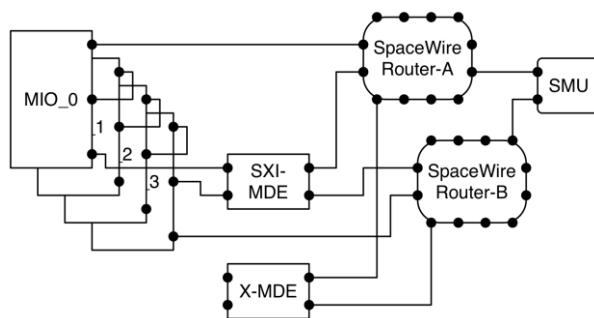
We have been working to design the SXI engineering model, which is a SpW/RMAP-based architecture of CCD driving and data handling using the SXI-PE and the SXI-DE. The block diagram of the SXI-PE processing unit is shown in Figure 4.

### 3.1 ARCHITECTURE

Here, we represent functions closely associated with SpaceWire/RMAP communication, while there are a lot of SXI-specific modules implemented in the User FPGA of the SXI-PE. In the current EM design of the MIO board, a relatively large-capacity memory (64 MByte SD-RAM) is connected to only the SpW FPGA.

However, the CCD data processed in the User FPGA need to be transferred to the memory. Therefore, to utilize an intervening (board-local) bus between User FPGA and SpW FPGA efficiently, we introduced buffering modules, “Bus I/F agents”, there. The Bus I/F agents have double buffers and regulate the data flow from the upstream to the downstream. Read and write from and to the double buffers are controlled by “Address manager”. When the one-sided buffer of the Bus I/F agent is filled with the processed data, the address manager switches the buffers’ I/O, sets the destination address, and triggers the data transfer to the target SD-RAM in accordance with established priorities of the stored data. The SXI-DE, on the other hand, access stored data in the SD-RAM by multiple RMAP read. The RMAP read is kept waiting by the SpW FPGA of the MIO while the target buffer memory is updating. The interface is “Exposure information” in the SD-RAM. After all the data transfer from the User FPGA to the SD-RAM is complete, the “Address Manager” unlocks the exposure information. HK data are collected during periodic intervals in the spare time.

### 3.2 SPACEWIRE NETWORK TOPOLOGY

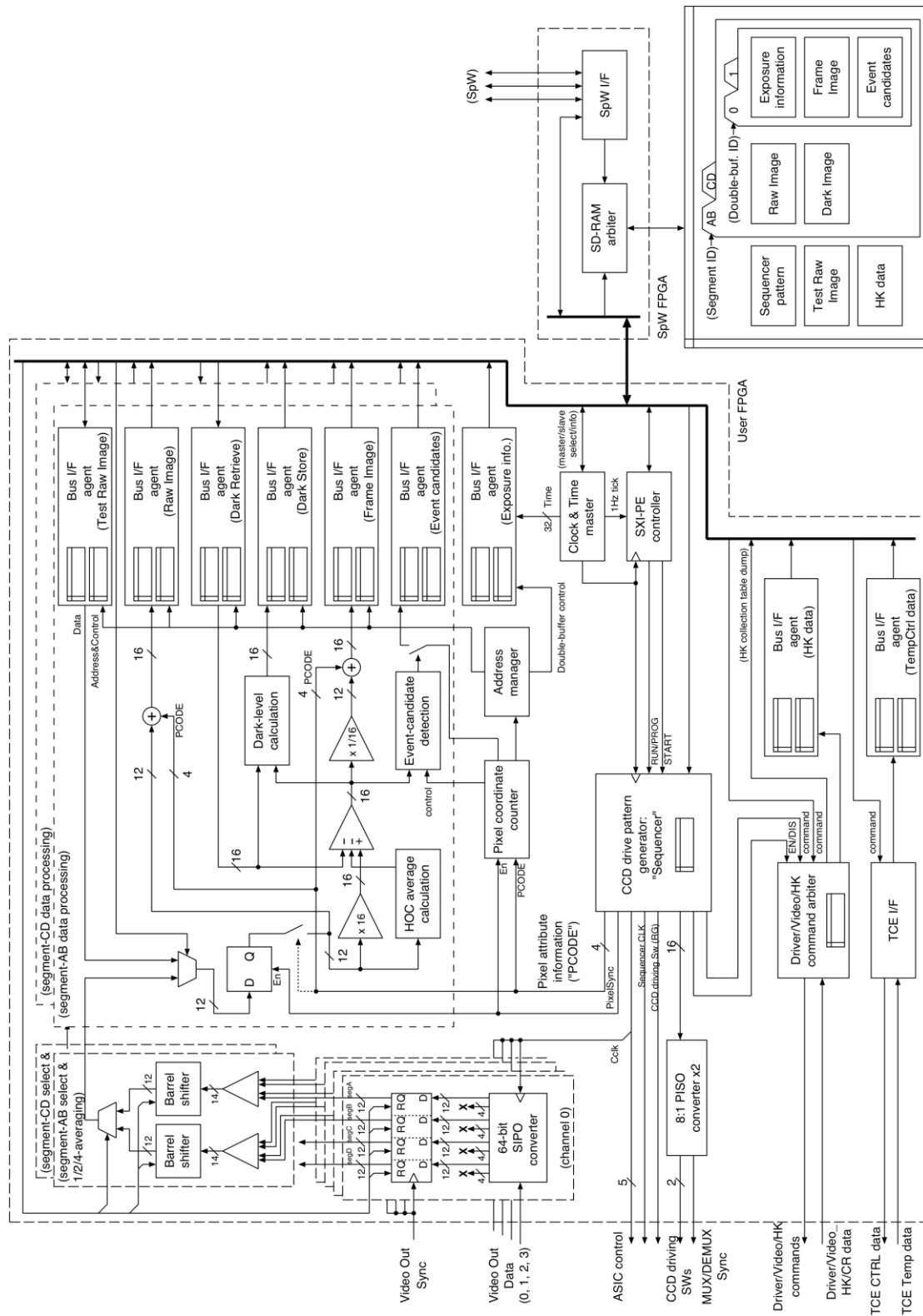


**Figure 3: SpaceWire network topology for the ASTRO-H SXI.**

We are also considering the SpW network topology for SXI to avoid single point of failure (SPOF) for the SXI-DE since SXI has only one CPU unit. Figure 3 shows the current design of the SpW topology to realize redundant configuration for the SXI system. Connecting at least two MIOs to SpaceWire routers (A and B), the route to use the common backup DE (X-MDE) via the SpW router is secured.

## 4 REFERENCES

1. Ozaki, M. et al. “NeXT SXI data processing system”, Proceedings of SPIE Space Telescopes and Instrumentation 2008: Ultraviolet to Gamma Ray
2. Ozaki, M. et al., “SpaceWire driven architecture for the ASTRO-H satellite”, this conference, 2010
3. Fujinaga, T. et al. “Development of SpaceWire based data acquisition system for the X-ray CCD camera on board ASTRO-H”, this conference, 2010.



**Figure 4: The block diagram of SXI-PE processing unit, which is for one CCD chip. Modules with the same function are displayed as layers.**