# A FAULT-TOLERANT SPACEWIRE COMPUTER

**Session: SpaceWire Onboard Equipment and Software**

**Long Paper**

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## ABSTRACT

A study of fault-tolerant on-board computers for satellite and payload control is described. The computer comprises duplicates of six different printed-circuit boards, for a total of 12 boards. Instead of using slow redundant buses such as 1553 or dual-CANbus, the 12 boards are interconnected with multiple SpaceWire channels, four per board. A packet-switched network using One doubly-connected torus topology provides at least two mutually-exclusive paths from each board to any other board.

## 1 INTRODUCTION

Space computers, as well as other electronic payload assemblies, typically comprise multiple printed circuit boards, interconnected by means of a backplane, and packaged in a ruggedized box. An example is shown in Figure 1. Often, two copies of each card are included and two parallel buses are employed, enabling dual module redundancy (DMR) and increasing the resiliency and the tolerance of a single failure.

Such systems, however, suffer of two key shortcomings. First, they are susceptible to multiple failures. Second, data rates of typical buses used in space applications, such as MIL-STD-1553 and CANbus, are too low for some applications. A novel system architecture, based on SpaceWire interconnect [1], is described in this paper. It enables higher data rates and offers an enhanced fault tolerance. The conceptual architecture is shown in Figure 2. The PCBs are still arranged linearly in a box, but the interconnect is based on multiple point-to-point SpaceWire cables arranged as shown in Figure 3.

## 2 BUS-BASED COMPUTER ARCHITECTURE

Figure 4 depicts a simplified single-bus architecture of a space computer, comprising five cards. A DMR version is shown in Figure 5, where each card is included twice in case one copy malfunctions. Usually, one or more of the cards manage the configuration and turn other cards on or off. At times, a dedicated reconfiguration management card is assigned with this task, and is constructed with internal redundancy to mitigate single point failures.

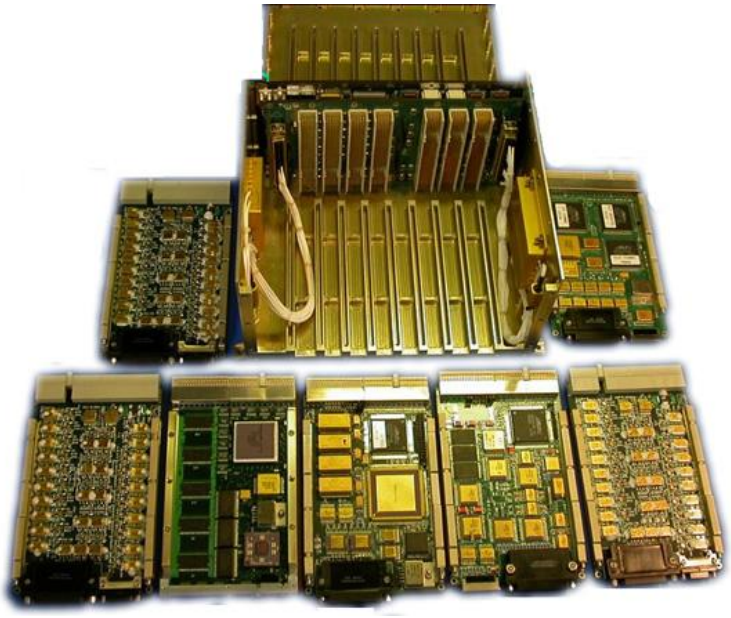

**Figure 1: A typical seven-card standard format space computer based on backplane interconnect**

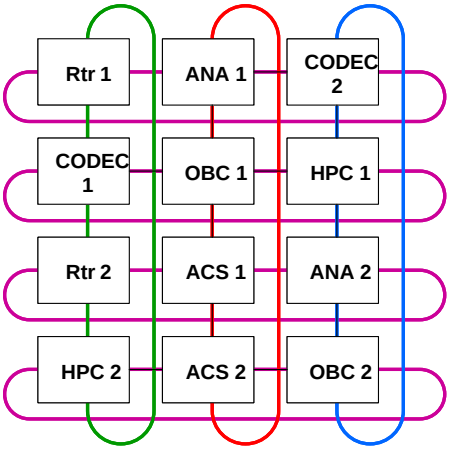


**Figure 2: The SpW Computer (**ANA: Analog I/O controller, CODEC: Communication port, OBC: On-board computer, HPC: High performance computer, ACS: Digital I/O controller, Rtr: Router**)**

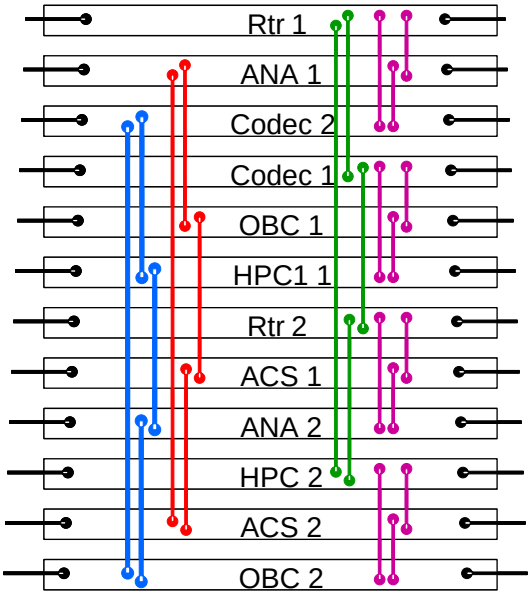


**Figure 3: Cards arranged linearly in a box**

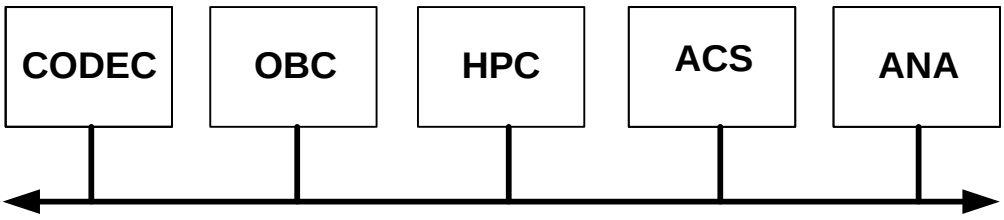


**Figure 4: A space computer**

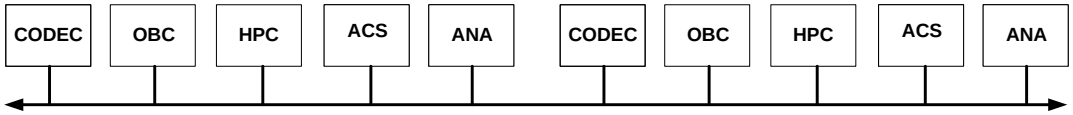


**Figure 5: Duplicating all cards of the space computer for DMR**

The structure of Figure 5 is still susceptible to a single failure in the bus. More reliable buses are enabled, e.g., by the MIL-STD-1553 standard which requires dual redundant buses, as in Figure 6 (1553 can also be implement with triple redundancy). Another common alternative is CANbus, implemented in duplicate similar to 1553 buses, used in order to take advantage of CANbus compatible components and to avoid export restrictions associated with 1553 components.

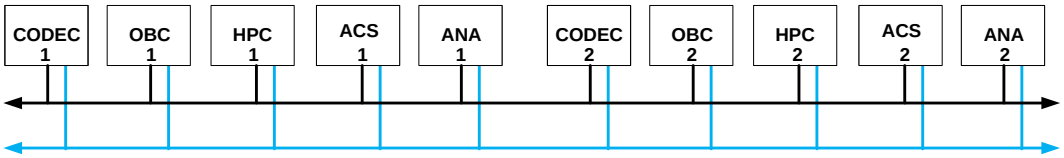


**Figure 6: Dual redundant bus (e.g. as in 1553)**

However, systems with dual buses are still sensitive to common failures. Indeed, a single module failure as in Figure 7 can be overcome thanks to the second copy of the failing card. However, the dual interconnect is more sensitive, because it is common to all units. If one of the two buses fails (Figure 8), the entire system is left with a single bus. Any additional failure on any of the ports, such as in Figure 9, may render the entire system unusable.

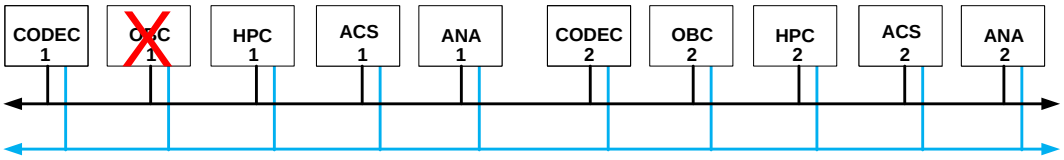


**Figure 7: The DMR dual bus computer is resilient to a single module error**

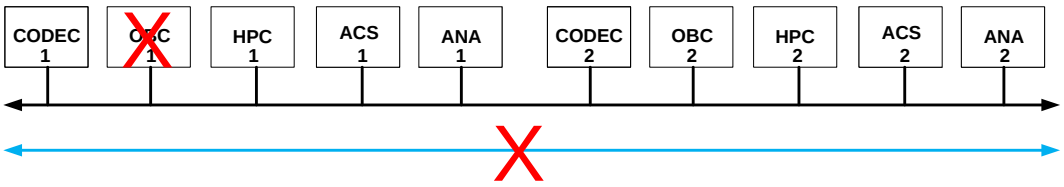


**Figure 8: A single bus failure eliminates bus redundancy**

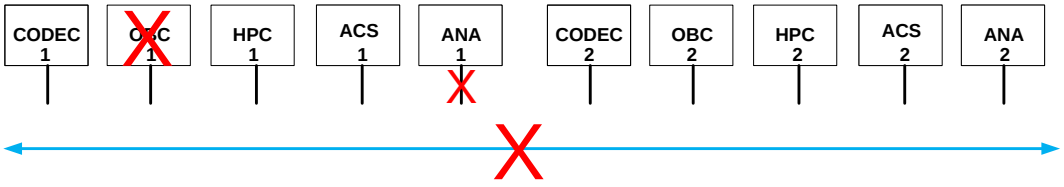


**Figure 9: A bus interface failure may disable the entire computer**

The other factor characterizing bus-based architectures is bandwidth limitation. Both 1553 and CANbus were designed mostly for the exchange of control data, rather than for the transfer of payload outputs or captured data. Both 1553 and CANbus are limited to 1 Mbit/s shared raw bandwidth, resulting in much lower effective sustained rates per node on the bus.

Avionics full-duplex switched Ethernet (AFDX) and various derivatives (ARINC) have been introduced as alternatives for aerospace applications. However, due to complexity and insufficient rates (about 1-2 Mbit/s at most), their use has been limited thus far. For high data rates, Ethernet requires special PHY components that complicates its application as a replacement for inter-board communications such as 1553 and CANbus.

## 3 THE SPW COMPUTER ARCHITECTURE

SpaceWire has been proposed as a high speed point-to-point link that enables creating redundant networks for replacing slow and fault-sensitive bus architectures [1]. The architecture of Figure 2 takes advantage of SpaceWire as the physical and data-link layers of a packet-switched network for use in multi-PCB computers. In addition to the 10 nodes of Figure 5, two extra routers are added, to increase connectivity within as well as outside the system. In packet switched networks, packets may have to pass through several intermediate nodes before arriving at its destination, and the intermediate nodes serve as routers or switches, merely passing the packet onward without affecting its contents. As common in such networks, upper layers of the network need to provide for routing, flow control, end-to-end control, reliability, retransmission, load balancing, configuration management in case of failures, and so on.

The network employs a doubly-connected torus topology (Figure 10, left). Each node is connected via four bi-directional ports, and every packet could be routed over any of the ports, creating redundancy of possible routing paths. A single node failure (Figure 10, right) results in shut-down of all four links incident upon the failing nodes; however, all other nodes remain connected.

A failure of one link causes it to disconnect without affecting the two end nodes (Figure 11, left). As above, such failure does not affect the functionality and availability of the system. In fact, many nodes and many links may malfunction and it is likely that the system will continue to perform its function, as demonstrated in Figure 11 on the right.

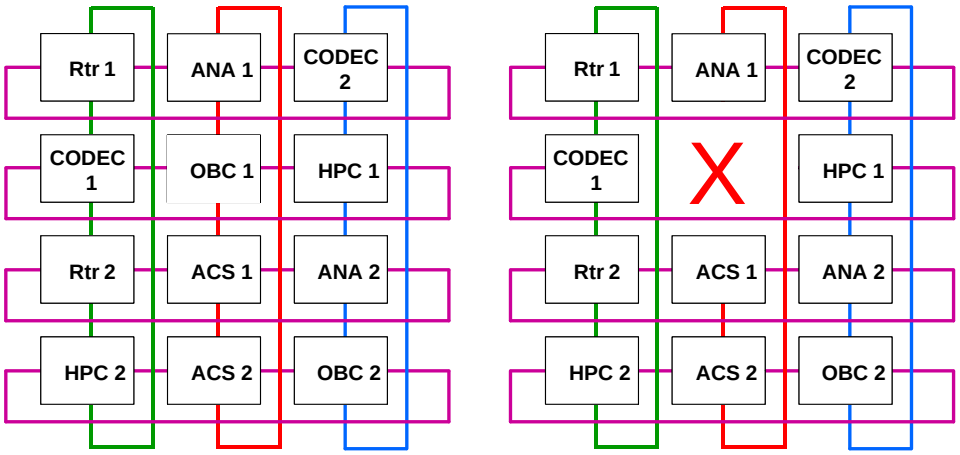


**Figure 10: SpW computer (left) after one node failure (right)**

Such a network-based computer systems can benefit from a multi-purpose computing-and-routing component as shown in Figure 12. Aeroflex Gaisler GR712RC is a system-on-chip (SoC) integrating two LEON3FT processor cores, large on-chip RAM and six SpaceWire ports, two of which implement the SpaceWire Remote Memory Access Protocol (RMAP, [2][3]). A typical board of the SpW computer (Figure 13) employs two copies of the SoC, one as the SpaceWire router and the other as either a main computer or as a controller managing other components on the board as well as external peripherals. The two RMAP ports of the router chip, as well as two other SpaceWire ports, make the four network connections. The remaining two ports can connect to the other processor chip (Figure 13) or to peripherals outside the SpW computer (Figure 14).

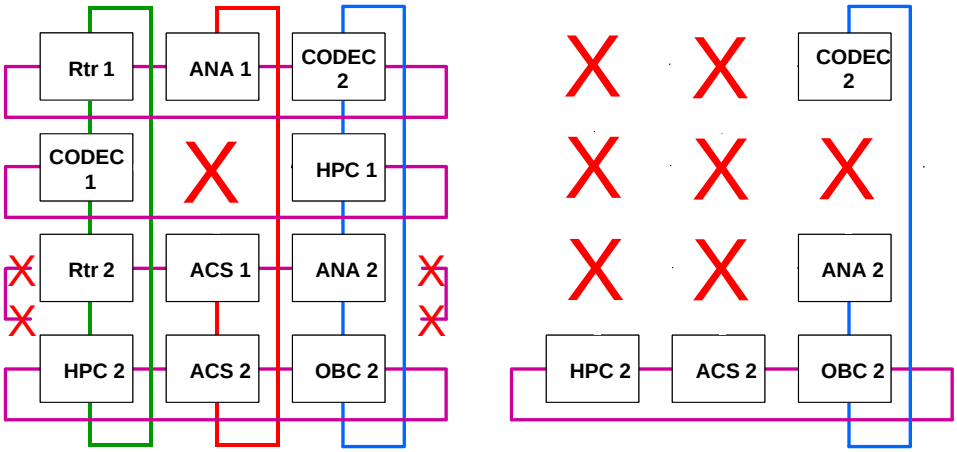


**Figure 11: SpW computer after one node and one wire failures (left) and after a maximal number of failures that still allow operation (right)**

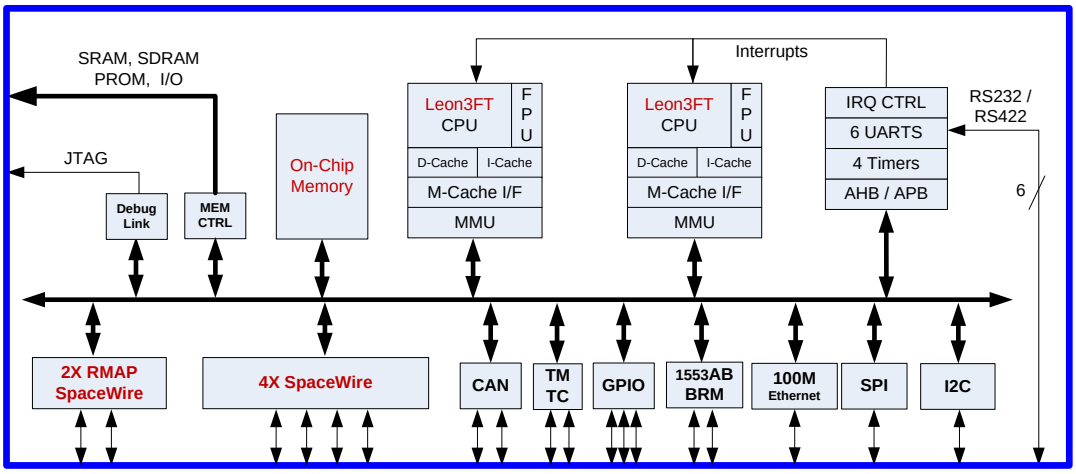


**Figure 12: Aeroflex Gaisler GR712RC SoC with six Spacewire ports can serve as a router, computer, or controller**

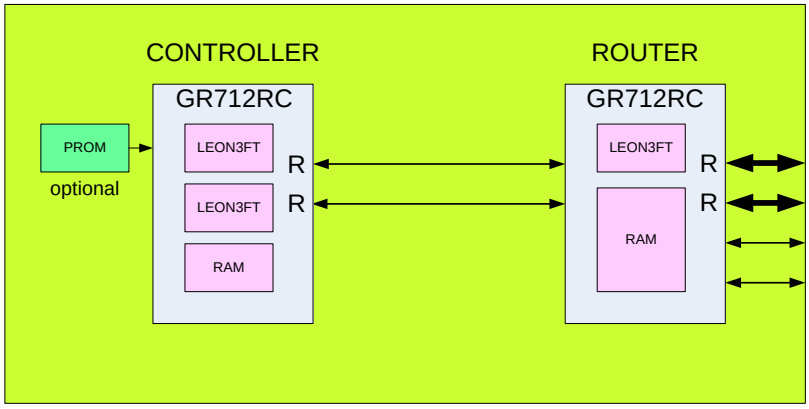


**Figure 13: Aeroflex Gaisler GR712RC SoCs serving as routers receive their code over RMAP links, use the on-chip memory and do not require local PROM or RAM chips. Router Processor boards may send code to other boards over RMAP SpW links. Controller boards may receive code over RMAP links, similarly to the routers**

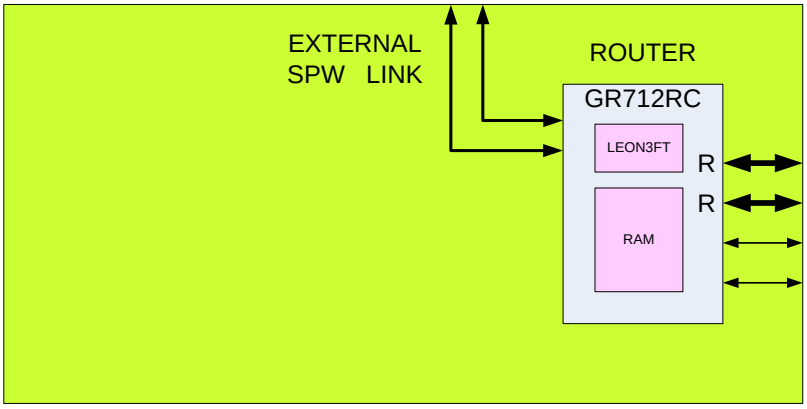


**Figure 14: One or two SpW links of the router chip may be used for external links to/from outside the SpW compuetr**

The advantage of RMAP ports is the ability to initialize the entire system from a single point (or two alternative points, for redundancy) as suggested in Figure 15. Thus, the network serves not only as a means of transferring data and control, but also to initialize, manage, test and repair itself.

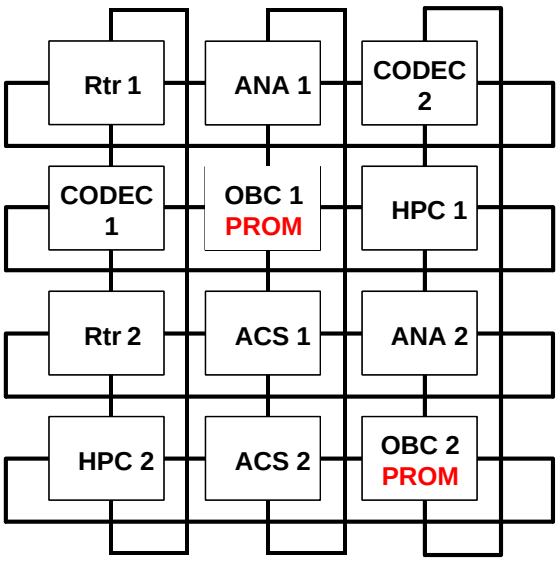


**Figure 15: Only two boards in this SpW computer carry PROM code and distribute the code to all other boards (routers and controllers) via RMAP SpW links**

SpaceWire links are typically designed to support up to 400 Mbit/s, providing a much higher bandwidth than any of the older buses described above. Given that in a network many (or even all) links may transfer data in parallel, the effective total bandwidth in the network described here is manifold higher than the bandwidth available in, for instance, the system of Figure 6. Even the scaled down network of Figure 11 (right) can deliver total combined bandwidth in excess of 1 Gbit/s. The actual bandwidth is typically limited by the software and by the architecture of the individual network nodes rather than by the network.

## 4 SUMMARY

The paper presents a SpW computer capable of high bandwidth and high level of fault tolerance. A doubly-connected torus topology offers a simple approach to the design of multi-PCB computer systems for space applications, and eliminates the need for older, slow fault-tolerant standard buses such as 1553 and CANbus.

Acknowledgements

The advice and ideas contributed by space engineering teams at the Technion, at Israel Aerospace Industries (MBT and Elta), at Ramon Chips and at Aeroflex Gaisler are greatly appreciated.

## 5 REFERENCES

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[3] S Habinc, M Isomeki, J Gaisler, The GRSPW SpaceWire Codec IP Core and Its Application, Int. SpaceWire Conference, 2007