EVOLUTION OF THE MARC SPACEWIRE AND POWER DISTRIBUTION ARCHITECTURE FROM CONCEPT TO TESTED HARDWARE

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Short Paper

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ABSTRACT

This paper describes the evolution of the Modular Architecture for Robust Computing (MARC) demonstration system from the initial design requirements to the developed and tested system hardware. The key design decisions to achieve the modular SpaceWire and power distribution network architectures are described with the supporting rationale. The network and power architectures are based on established spacecraft redundancy concepts and provide tolerance to single point failures. The MARC hardware has been tested and the capabilities, facilities and test results are summarised.

1 INTRODUCTION

The Modular Architecture for Robust Computing (MARC) [1] demonstration hardware is a modular processing system for implementing spacecraft payload and platform avionics.

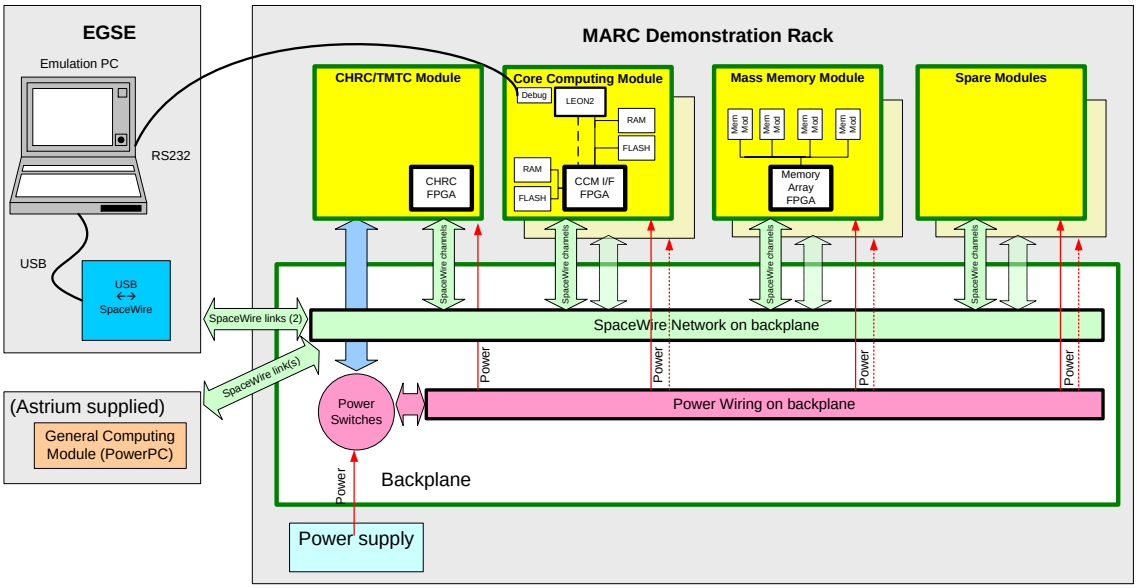

Figure 1: MARC demonstration system

MARC employs a distributed hardware architecture incorporating modules that are interconnected by a SpaceWire network; this design simplifies resource sharing (e.g. computing, communication network, memory, etc.) amongst the payload and platform functions. The main applications foreseen for this architecture include missions requiring extensive distributed fault-tolerant on-board processing capabilities, such as advanced payload data processing systems and highly autonomous space exploration systems.

A SpaceWire Active Backplane (SpWAB) [2] provides the network connections to support a set of Modules. The network can be expanded to support additional Modules or to meet the performance requirements for a particular mission. The SpW interfaces implemented in the MARC system modules use the recently released ESA RMAP IP Core [3] and the SpWAB uses the Atmel AT7910E 8 port router.

The reliable computing resource in MARC is provided by two Core Computing Modules (CCM) based on the Atmel AT697F processor. The hardware is designed to support the software architecture and the services based on the Spacecraft Onboard Interface Services (SOIS) standards.

2 MARC SpW Network Architecture

There are a variety of classical network architectures that were considered for the SpW network as illustrated in Figure 2. In this diagram the green spots could represent either a functional Module or a router. Any of these architectures could be adopted however each has advantages and disadvantages in differing applications.

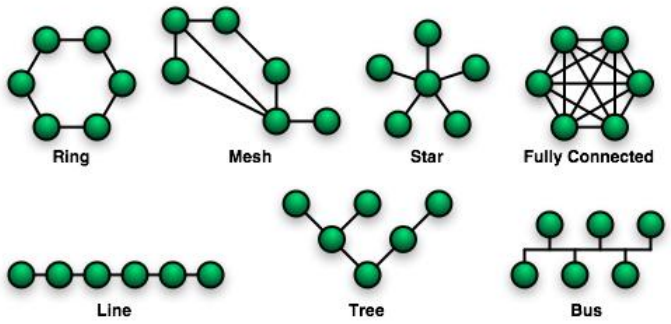

Figure 2: Classical network architectures

Single Point Failure (SPF) avoidance requires each MARC Module must connect to 2 independent routers, thus a modular network building block can be created that is naturally composed of 2 routers. In the MARC system this building block is called a "Cluster" and larger networks can be created by linking clusters (Figure 3). In principal the clusters may themselves be linked together in a variety of architectures, for example each green spot in Figure 2 could represent a Cluster. Within spacecraft practical considerations normally limit the number of Modules that need to be supported and so the simple redundant bus network architecture adopted for MARC is adequate. To support spacecraft integration and test activities spare ports are available to interface with Electrical Ground Support Equipment (EGSE). Additional spare ports are provided to connect to other external functions.

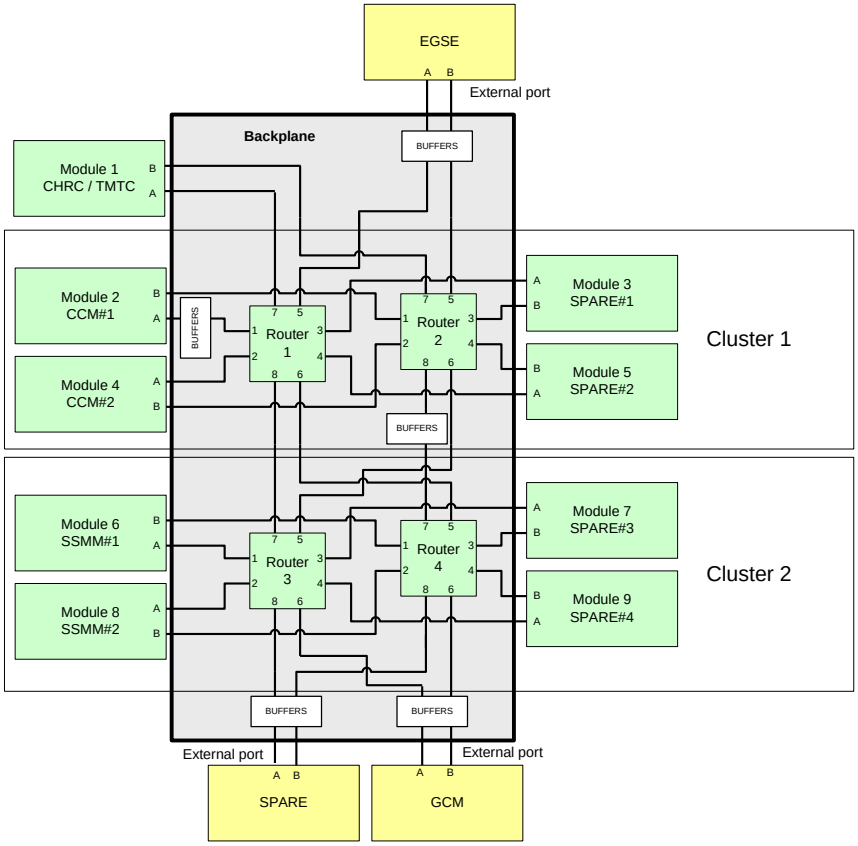

Figure 3: MARC demonstration system Cluster based SpW network architecture

3 FAILURE DETECTION ISOLATION AND RECOVERY

Failure Detection Isolation and Recovery (FDIR) autonomy is essential for space missions, in particular where recovery has to be performed without ground intervention. This is implemented by a combination of hardware and software [4]. The FDIR hardware element within MARC is the Core Hardware Reconfiguration Controller (CHRC), this is responsible for ensuring that key SpWAB routers are powered and that at least one master CCM is running. The correct functionality of the master CCM and the FDIR Manager Software running within it is indicated to the CHRC by regular SpW heartbeat messages that reset a watchdog timer in the CHRC. The objective of the CHRC FDIR action is to power a master CCM with a working communications path to the CHRC. If the CHRC fails to do this successfully it will flag the problem to the ground operator via a connection with the Telemetry and Telecommand sub-system.

4 POWER DISTRIBUTION ARCHITECTURE

It is anticipated that during a mission the MARC system will be operated in a variety of configurations that employ a subset of the available routers and Modules, this means that each router and each module must have an independent power switch. These power switches are controlled by the CHRC to permit the hardware controlled FDIR actions to be accomplished either automatically or by telecommand. To mitigate against SPFs the power distribution architecture must be comprised of Nominal and Redundant power feeds with over-voltage and over current protection [5]. The derived MARC power distribution architecture is shown in Figure 4.

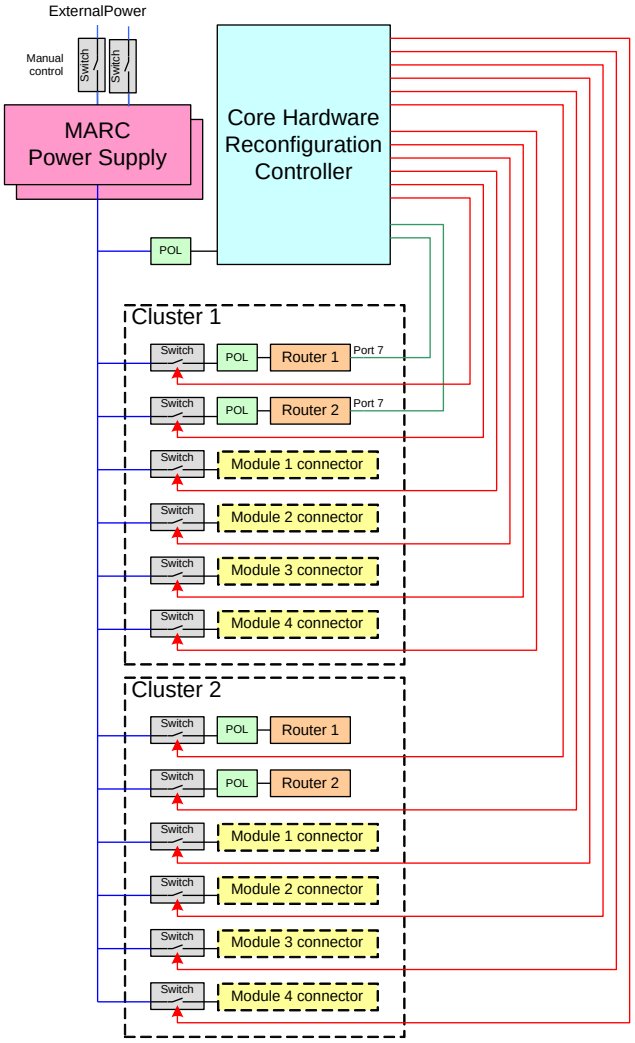

Figure 4: MARC demonstration system power distribution and control architecture

5 MARC DEMONSTRATION RACK AND TEST RESULTS

The MARC demonstration hardware (Figure 5) was completed and tested in 2009, it comprises:

- A 9U case and 6U card frame
- A SpW Active Backplane
- One Core Hardware Reconfiguration Controller Module
- Two Core Computing Modules
- Two Mass Memory Modules
- Four spare Module slots
- Rack power supplies

The ESA RMAP IP Core has been implemented in Actel ProASIC 3 devices and operates at 100Mbps (180Mbps maximum predicted by design tools).

The MARC Rack has been tested and is fully operational. The measured power dissipation figures are listed in Table 1.

Figure 5: MARC demonstration system

Module	Power	Qty	Total Power
Backplane (All links 100Mbps)	19W	1	19W
Core Computing Module	12W	2	24W
Solid State Mass Memory Module (2 x SSMBMs)	14W	2	28W
Core Hardware Reconfiguration Controller	0.5W	1	0.5W
		Total	**~72W**

Table 1: Power dissipation of the MARC demonstration system

6 REFERENCES

1. A. Senior, P. Ireland, S. Fowell, R. Ward, O. Emam, B. Green, “Modular Architecture for Robust Computing (MARC)”, International SpaceWire Conference 2007.

2. A. Senior, P. Worsfold, W. Gasti, “A SpaceWire Active Backplane Specification for Space Systems”, International SpaceWire Conference 2010.

3. C. McClements, S. Parkes, "ESA/Dundee SpaceWire RMAP Core", International SpaceWire Conference 2010.

4. A. Senior, W. Gasti, O. Emam, T. Jorden, R. Knowelden, S. Fowell, “Modular Architecture for Robust Computation”, International SpaceWire Conference 2008.

5. F. Tonicello, M. Triggianese, "Points of Load Converters and distributed power architecture approach", ESA Technology Innovation Day, February 2010.