VALIDATION AND TESTING OF AN IP CODEC FOR HIGH BANDWIDTH SPACEWIRE LINK[1]

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Short Paper

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ABSTRACT

In this paper we present the design, development and testing of a SpaceWire codec that is fully compliant with ESA standard ECSS-E-ST-50-12C. This codec is part of the high bandwidth communication infrastructure employed in the Spanish INTA Microsat satellites programme. Four FPGAs families have been used to validate our design. Three of these implementations have been tested against commercial solutions using a suite of utilities developed within our group. With these utilities, the user is able to configure the hardware, transfer data and check the status of the SpaceWire links. The results of all tests are presented, including real performance results and compatibility test results.

1 INTRODUCTION

The Space Research Group of the Universidad de Alcalá has developed a SpaceWire IP Codec that allows a high bandwidth data exchange through a SpaceWire link. The initial motivation for the development of this IP Codec was to satisfy the data communications requirements for the Energetic Particle Detector (EPD) onboard Solar Orbiter [1]. It is also planned to use it within the MicroSAT satellites programme, which belongs to the Spanish Instituto Nacional de Técnica Aeroespacial (INTA) [2].

In the process, the Codec has been developed for four FPGA families, namely Spartan3E and Virtex4 from Xilinx and ProASIC3E and Axcelerator from Actel. Several tests have been carried out for most of these families, including compatibility with existing commercial solutions from Star Dundee and Gaisler Research, data transfer rate and data integrity tests.

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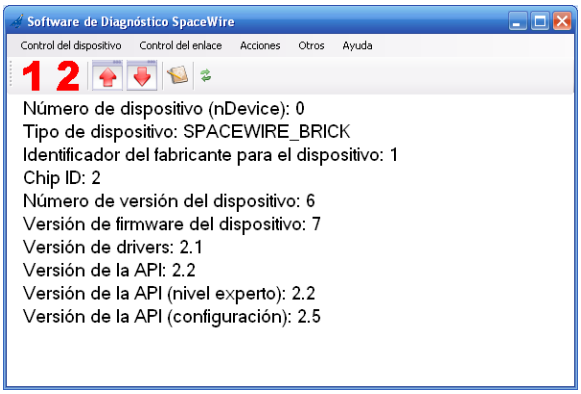
In this paper, the results of all tests made are available, as well as occupation information for the SpaceWire Codec developed by our group compared to similar products developed by others.

2 TESTING ENVIRONMENT

To carry out the aforementioned tests, our SpaceWire Codec was tested against three commercial solutions: Star Dundee's SpaceWire PCI-2, Star Dundee's USB Brick and Gaisler Research's RTC Development Suite.

For controlling both of Star Dundee's solutions, a Microsoft Windows diagnostic application was developed by our group. It allows the user to configure the hardware, send and receive data, perform loopback tests, as well as get information about the status of the SpaceWire links and data transfers. The main screen of the application is shown in the figure on the right side of these lines.



For performing the tests against the Gaisler Research's RTC, several applications have been developed for the RTEMS Operating System [3]. These applications allow sending and receiving data over a SpaceWire link, measuring the time used to carry out the transmission and comparing data sent and received so that they are equal, allowing for a data integrity test. A screen capture of the application is shown in figure 1.

```
grlib> load t
section: .text at 0x40000000, size 128064 bytes
section: .data at 0x4001f440, size 2784 bytes
total size: 130848 bytes (87.8 kbit/s)
read 743 symbols
entry point: 0x40000000
grlib> run
******** Starting SPW TX TEST ********
LINK_STATE[SPW0]: 5 - RUN
SpaceWire Transmission FINISHED: 16387,2 Mb in 133.0000 s [123.2120 Mbs]

Program exited normally.
grlib>
```

Figure 1: Application for controlling Gaisler Research's RTC.

3 TEST RESULTS

For testing and validating our IP Codec implementations, three kind of tests were carried out:

a) PC/RTC to FPGA and FPGA to PC/RTC data transmission: This test allows to determine the maximum data rate achievable. The FPGA is programmed with our SpaceWire CODEC, plus a component that generates data and sends it through the SpaceWire Codec, and a data receiver component which reads the data that arrives from the SpaceWire link through the Codec.

In this test, a stream of data is sent from the PC/RTC or FPGA to the other end of the link, and the time it takes to transfer the data is measured.

b) Data Integrity test: For this test, the FPGA is programmed with our SpaceWire Codec, plus a FIFO Buffer and an interface component. This interface component has two tasks: first, it reads data that arrives from the SpaceWire link through the Codec and stores it in the FIFO Buffer. When there is data available in the buffer, this component reads it and sends it through the Codec.

   In this test, a PC sends several fixed-sized packets through the SpaceWire link, filled with random data. The IP Codec resends the data to the PC upon reception. In the PC, the data received is compared with the data sent to check if there are errors.

c) Loopback test: This test is similar to the first one, but the Codec outputs are connected with its inputs. This allows to determine the maximum operating frequency of the Codec. Also, when sending data through the link, it allows to determine the maximum data rate for simultaneous transmit and receive operations.

General testing results are presented on figure 2.

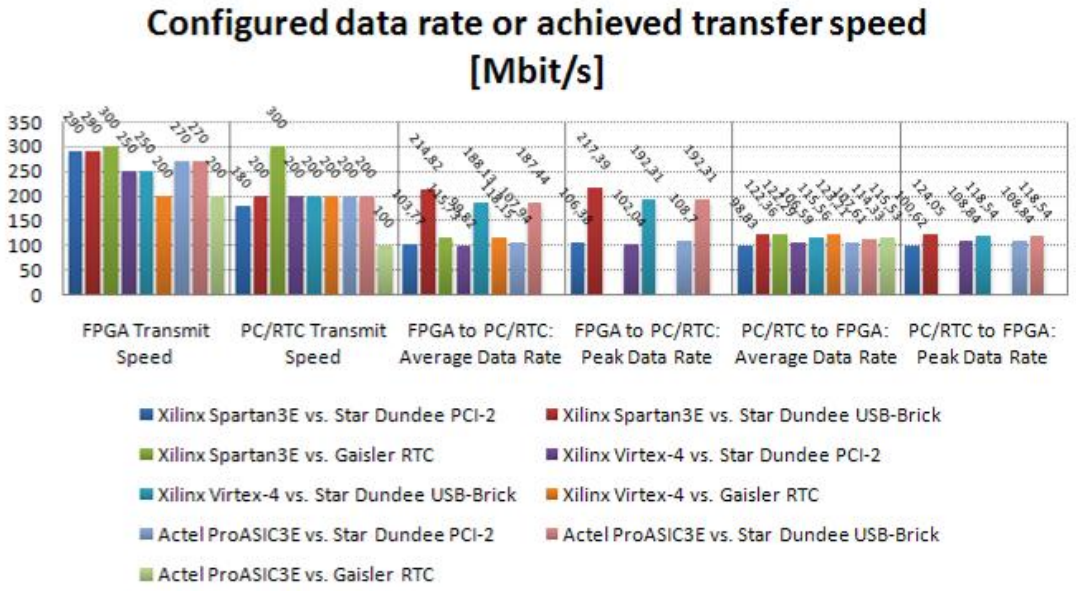


Figure 2: SpaceWire IP Codec test results

Other tests were also carried out for the Xilinx Virtex4, Xilinx Spartan3E and Actel ProASIC3E implementations:

- Data Integrity: Test carried out successfully on all implementations, transferring and comparing 25.000 packets of 21.844 bytes each.

- Loopback Test: Link established successfully on all implementations, with a transmitter speed of 290 Mbit/s for Xilinx Spartan3E, 250 Mbit/s for Xilinx Virtex4 and 270 Mbit/s for Actel ProASIC3E. Data throughput was measured

to be 218,45 Mbit/s for Spartan3E, 190,512 Mbit/s for Virtex-4 and 204,8 Mbit/s for ProASIC3E.

- Post Place&Route Simulation: Two instances of the FPGA design explained in the data transmission test were tested against each other. A SpaceWire link was established successfully on all implementations, at 300 Mbit/s for Spartan3E, 400Mbit/s for Virtex4 and 270 Mbit/s for the ProASIC3E implementation. Exchange of data was carried out normally in all cases.

3.1 ACTEL AXCELERATOR

This implementation has only been tested on post-layout simulation. Two instances of the FPGA design explained in the data transmission test were tested against each other at 200 Mbit/s. A link was established successfully and a transfer of a 20480 byte packet took 1075,761 µs, which results in a data rate of 152,301 Mbit/s.

4 OCCUPATION DATA

In figure 3, the reader can find the occupation data for the four implementations of the SpaceWire Codec, as well as data for alternative solutions from AeroFlex Gaisler and ESA. Information from Star Dundee is also shown below. Please keep in consideration that the data from these alternative solutions could also include additional functionality besides the SpaceWire Codec.

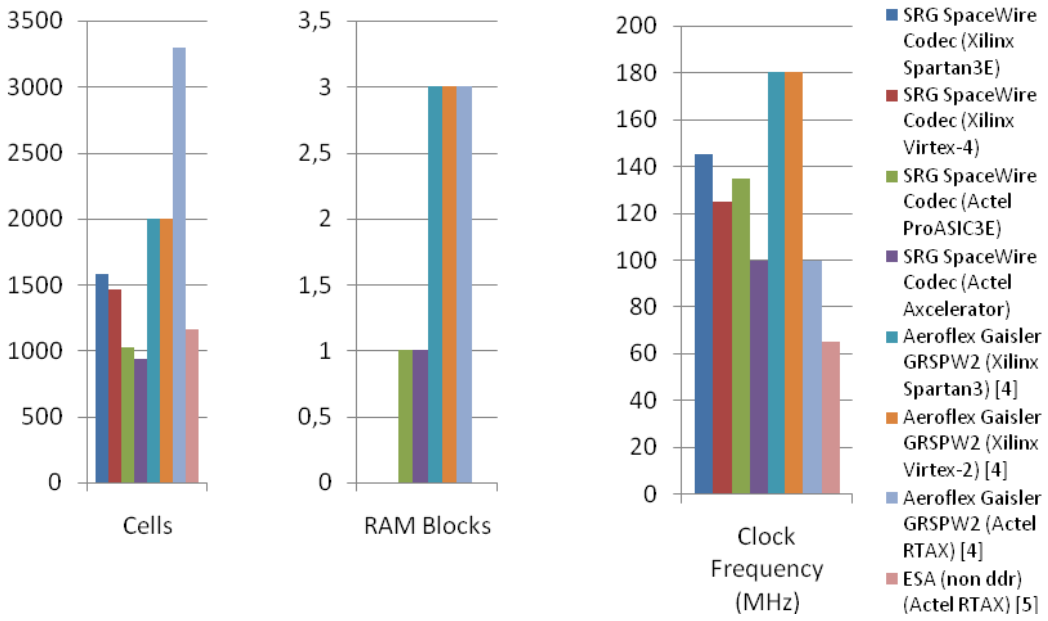


Figure 3: SpaceWire IP Codec occupation data

- Star Dundee [6]: Approximately 7% of an Actel RTAX1000 or 4% of a Xilinx Spartan3E 1600

5 CONCLUSIONS AND FUTURE WORK

A SpaceWire IP Codec has been developed for four of the most used FPGA families, which allows for a high bandwidth point to point data exchange. Compatibility tests of our SpaceWire Codec with current commercial alternatives have been carried out

successfully, reaching data throughputs of up to 217,39 Mbit/s on a Xilinx Spartan3E, 192,31 Mbit/s on a Xilinx Virtex-4 and 192,31 Mbit/s using an Actel ProAsic3E. On simulation, an Actel Axcelerator implementation reached 152,301 Mbit/s.

Work is in progress to enhance the IP Codec's functionality, adding support for Packet Routing, RMAP [7] and CCSDS [8], as well as increasing the maximum operating speed, especially for the Xilinx Virtex implementation where the maximum operating frequency in simulation was greater than the maximum frequency achievable for a normal operation in the FPGA implementation.

6 REFERENCES

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