IMPLEMENTATION OF A DYNAMICALLY RECONFIGURABLE PROCESSING MODULE FOR SPACEWIRE NETWORKS

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Short Paper

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ABSTRACT

The ESA-project "FPGA based generic module and dynamic reconfigurator" targets the development of a hardware architecture, called DRPM (for Dynamically Reconfigurable Processing Module). The goal of the DRPM is to develop a system that allows for the adaptation of hardware components in flight at run-time. This is enabled by the implementation of an SRAM-FPGA-based partially reconfigurable core, which is embedded into a system hosting a reconfiguration controller and a system controller providing suitable interfaces for space applications. Maximum flexibility is realized by implementing SpaceWire interfaces that enable the DRPM integration into a SpaceWire network. Moreover, the SpaceWire RMAP protocol is used for remote access to registers and memory banks of the DRPM.

1 INTRODUCTION

One of the main advantages of the SpaceWire protocol is the reusability of already developed SpaceWire-based memory units and payload processing components. The reusability does not only reduce the development costs, but also improves the reliability of the systems. Therefore, there is a need for increasing the reusability of already developed payload processing components for future missions. With respect to hardware devices, SRAM-based FPGAs offer reconfigurability, which allows for the development of generic payload processing modules. The use of generic modules in a space environment has numerous advantages. In terms of system-specific hardware, a reconfigurable generic module can ensure maximum reuse of development across different systems. Since high development costs are usually incurred during custom FPGA development, a more modular approach can be used with only custom modules being added as peripheral systems within the FPGA.

Current and upcoming application specific standard products (ASSPs) offer limited processing performance, which require multiple device instances in many cases to support the high data rates provided by current sensors. In contrast to ASSPs, FPGAs are advantageous for common high data rate applications like image processing, compression, and generic signal processing. Compared to general purpose processors, FPGAs often offer a better performance and more adaptability, particularly for applications where a parallelized algorithm can be implemented on the FPGA.

Reconfigurable hardware allows payload processing to be changed or adapted during a mission. Therefore, systems can be freely adapted to every possible scenario, even if it was not foreseen at design time. Moreover, if the devices can be reconfigured dynamically, this adaptation can also be done in an efficient manner during run-time, where parts of the device can remain operative, whilst others are changed. This allows for implementing time-sharing of the reconfigurable resources between different applications, thus increasing the area efficiency.

The following sections show the DRPM in detail, emphasizing its SpaceWire functionality, which is core to the DRPM concept in terms of payload system integration. The SpaceWire capabilities of the DRPM are also complemented by additional interfaces for directly accessing high speed instruments.

2 DYNAMICALLY RECONFIGURABLE PROCESSING MODULE

The focus of the project is on the development of the reconfigurable core including its control mechanisms. The DRPM demonstrator aims at showing the capabilities of the reconfigurable core by executing different payload processing applications on the same hardware. Concerning the harsh space requirements, mitigation of radiation effects and recovery in case of failure is emphasized.

The DRPM features several SpaceWire interfaces for avionics and instrument source data allowing for the DRPM to be integrated into a SpaceWire network as general purpose processing node. The DRPM supports the SpaceWire remote memory access protocol (RMAP) [1] in order to enable access to the registers and memory banks of the DRPM from other nodes in the SpaceWire network. The SpaceWire RMAP functionality allows for access to the working memory of the payload processing components as well as access to the program and configuration memory. This is useful for debugging purposes or remote uploading of new software applications or FPGA configuration files.

Besides its SpaceWire connectivity, the DRPM features additional dedicated instrument interfaces, ranging from high rate instruments interfaced via WizardLink to lower rate instruments interfaced via CAN bus, discrete I/O and legacy serial links such as e.g. RS422. Instrument control may be performed according to an instrument’s specific needs, which may include control via SpaceWire, CAN bus or customized discrete interfaces. As an alternative to SpaceWire the avionics can be connected via MIL-STD-1553B. The DRPM contains a partially reconfigurable core that allows for customized interfaces to be tailored depending on specific needs. The main feature of the partially reconfigurable core, however, is to allow for high performance data processing algorithms to be implemented to cover a wide range of applications. In addition, it shall support in-flight reconfiguration during a mission where required, whilst being fault-tolerant to space environment effects typically

caused by high energy particles. A demonstrator platform of the DRPM is being developed, which is used for system exploration. It is based on the rapid prototyping system RAPTOR [2] and features all required hardware components and interfaces. Fault injection mechanisms, which emulate effects such as single event upsets, are used to verify the fault-tolerance features of DRPM.

3 PARTIAL FPGA RECONFIGURATION

The DRPM consists of partially reconfigurable FPGAs (PR FPGAs), which are used for the payload processing. When utilizing partial reconfiguration suitable design methods are required for partitioning the FPGA resources. In the DRPM a tiled partially reconfigurable region as described in [3] is used, where the FPGA area is divided into a static region and a partially reconfigurable region (PR region). The static region contains system components that are constantly active, while the PR region is reserved for dynamic system components, which are referred to as partial reconfiguration modules (PR modules). PR modules can be loaded and unloaded at run-time according to the needs of the application. The partial reconfiguration is performed by a dedicated reconfiguration controller, which transfers the configuration files from the PR module storage to the configuration interface of the PR FPGA. In order to mitigate single-event upsets (SEU), hardening techniques such as triple modular redundancy and configuration memory scrubbing are applied.

4 SYSTEM EXPLORATION

In the following, two example systems are introduced, which can be realized by the DRPM demonstrator platform. Both systems feature avionics and source data interfaces as specified in Section 2. The building blocks are the SpaceWire RTC AT7913E, one or more partially reconfigurable FPGAs (PR FPGAs), and a communication FPGA (COM FPGA), which is used to interconnect the SpaceWire RTC and the PR FPGAs.

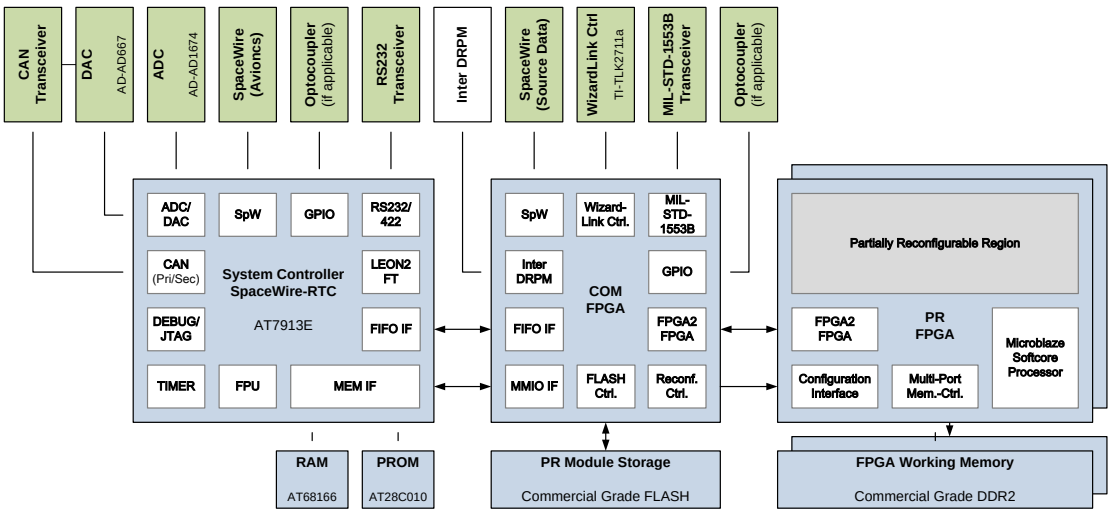

Figure 1 DRPM with external device interface control via the COM FPGA.

In the first system, shown in Figure 1, the interface control is implemented in the COM FPGA. It includes source data instrument interface controllers, such as 4 SpaceWire RMAP IP Cores [4], a Wizard-Link controller, general purpose IO, and a

MIL-STD-1553B controller. The system controller is connected via a FIFO and a memory mapped IO interface. The COM FPGA implements a Flash controller to gain access to the PR module storage. The reconfiguration controller is used to apply full and partial reconfiguration of the PR FPGA. The inter DRPM interface allows a connection to additional DRPMs. The second system, which is shown in Figure 2, implements the interface control on the PR FPGA. The only components, which are implemented on the COM FPGA are the FIFO interface to the system controller, the reconfiguration controller, and the corresponding configuration memory controller. In comparison to the external device interface control, the self-hosting interface control allows for a closer coupling between source data interfaces and the PR modules used for payload processing. The self-hosting interface control requires fewer resources on the COM FPGA, but more resources on the PR FPGA.

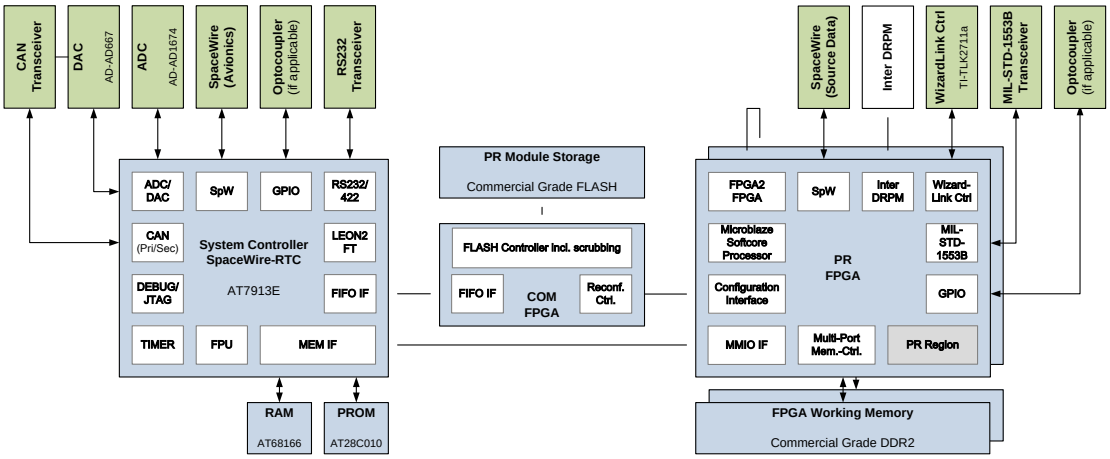

Figure 2 DRPM with self-hosted interface control on the PR FPGA.

5 CONCLUSION

In the current state of the project, the hardware and software components of the DRPM demonstrator are under development. One of the main features is the utilization of dynamically reconfigurable FPGAs, which are used for high performance payload processing. The SpaceWire RMAP protocol is used to remotely control the DRPM in a SpaceWire network. The flexibility of the DRPM demonstrator helps identification of different system architectures for space applications. Thus, various systems can be prototyped and analysed before defining the final architecture, which is considered for flight use.

6 REFERENCES

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