IMPLEMENTING SPACEWIRE RMAP LINKS IN FLASH-BASED FPGA TECHNOLOGY

Session: SpaceWire Components (Poster)

Short paper

Sandi Habinc, Jonas Ekergarn, Kristoffer Glembo

Aeroflex Gaisler, Kungsgatan 12, SE-411 19 Göteborg, Sweden

sandi@gaisler.com, ekergarn@gaisler.com, kristoffer@gaisler.com

ABSTRACT

Aeroflex Gaisler (Sweden) is developing the software and the digital part of a Motion Control Chip (MCC) in an activity that is lead by ÅAC Microtec (Sweden) under a contract with the European Space Agency (ESA). The digital logic is implemented in a Flash-based FPGA, including SpaceWire [1] RMAP [2] interfaces.

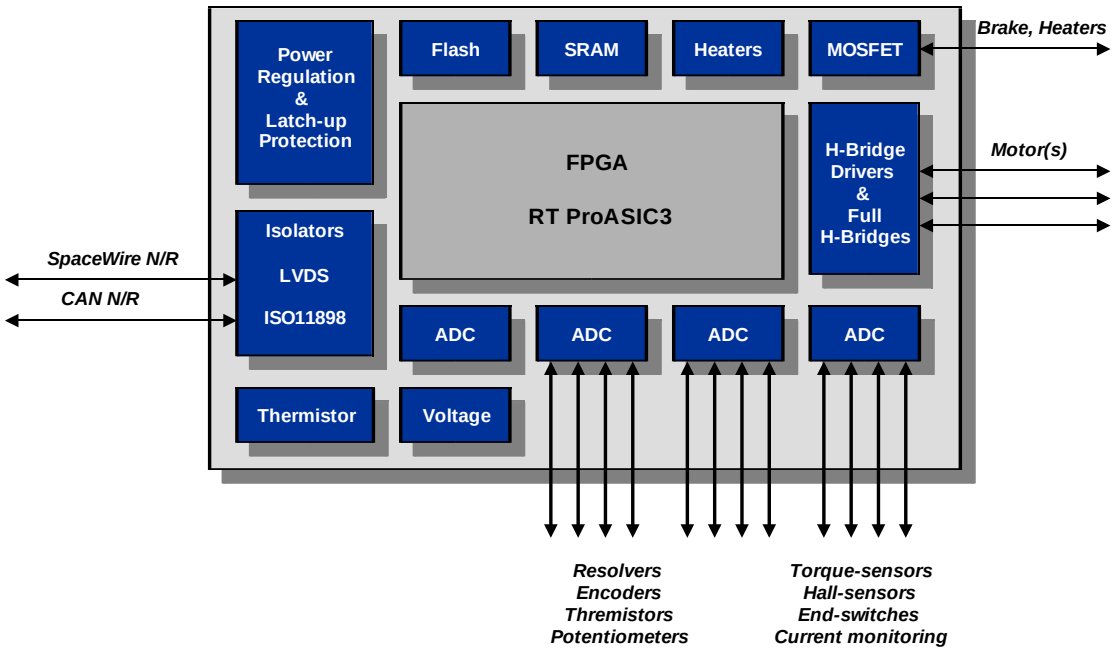
OVERVIEW

The Motion Control Chip (MCC) is a freestanding component that can control up to three brushed motors or one brush-less motor in torque, position or velocity mode, and will be implemented as an advanced 3D-multi-chip-module (3D-MCM) [3].

The baseline design includes a field programmable gate array (FPGA) as a naked die for the implementation of the digital part. To allow for programmability and future enhancements, a re-programmable FPGA has been selected.

The choice of a re-programmable over a one-time programmable FPGA has been driven by various factors, the two most prominent being that the 3D-MCM should be possible to program to different customer's needs and that qualification of programming procedures for one-time programmable FPGAs as a naked die is not straightforward.

Figure: Block diagram of MCC



FUNCTIONALITY OF FPGA

1.1 OVERVIEW

The digital design forms a system-on-a-chip comprising key elements such as the fault-tolerant LEON3-FT 32-bit SPARC processor [5], optional floating-point unit, debug support unit, etc. The main interfaces of the FPGA are listed hereafter:

- SpaceWire link with optional RMAP to support remote memory access for software download and debug, based on ECSS standards
- Optional redundant CAN 2.0A/B bus interface, based on ECSS standards
- SPI interface for access to ADC devices, support for multiple accesses in parallel to allow correlations
- Pulse Width Modulation: symmetric and asymmetric
- General Purpose Input Output
- Memory Controller with EDAC to protect external PROM & SRAM memory
- JTAG Debug Link, used for software download & debug

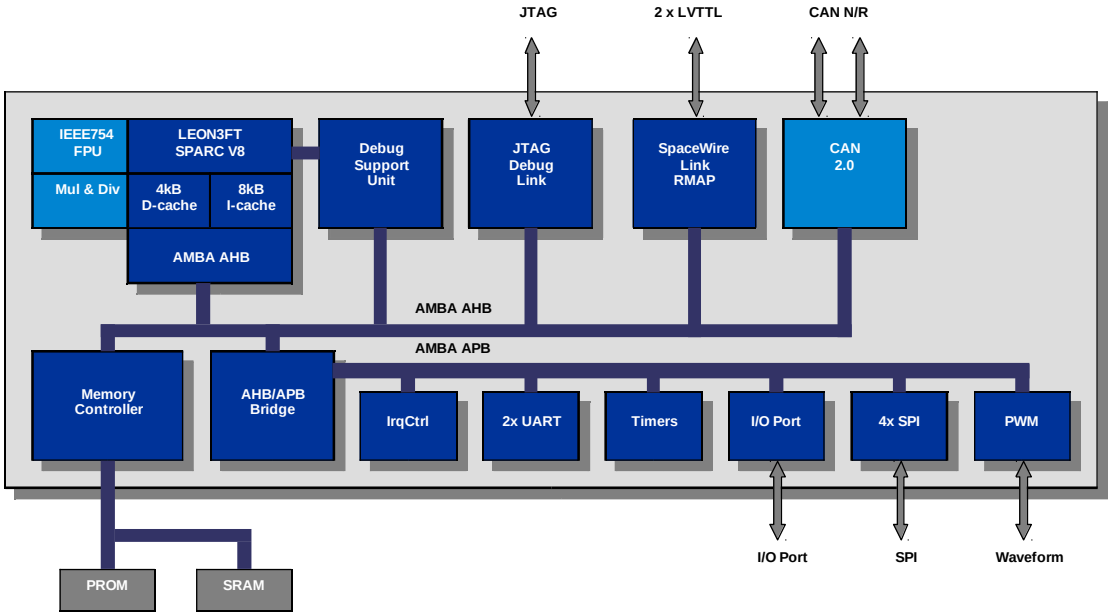


Figure: MCC FPGA block diagram

1.2 FPGA TECHNOLOGY

The Actel ProASIC3 RT3PE3000L FPGA part has been chosen for the implementation of the digital logic. Although this part can tolerate a total ionizing dose (TID) of up to 20 krad and is basically single event latch-up (SEL) free, it exhibits some sensitivity to single event upsets (SEU) and transients (SET) that needs to be taken into account during logical design.

Main features of the Actel RT3PE3000L FPGA are listed hereafter:

- 3,000,000 System Gates
- 75,264 Logic Tiles
- 504 kbits RAM
- 1 kbits FlashROM (user accessible)
- RT ProASIC3 use same process as commercial UMC 0.13 µm ProASIC3EL
- RT3PE3000L is the same silicon as the A3PE3000L

1.3 IMPLEMENTATION APPROACH

The MCC FPGA has been designed using the same IP cores that are used by Aeroflex Gaisler in their LEON3FT-RTAX product line that is based on Actel's RTAX2000S anti-fuse FPGA parts. The portability of the IP cores, all written in VHDL, permits a move from anti-fuse to Flash based FPGA technology with a minimum of effort [4].

The on-chip block memories have been protected against SEUs using either error correction and detection (EDAC) or simple parity code for the detection of bit errors. The flip-flops have been protected against SEUs using triple modular redundancy (TMR) that can be automatically inserted by the VHDL synthesis tool.

The probability of SETs in combinatorial logic at modest clock frequencies (25 MHz) is very low, according to reports from Actel, which should not require any mitigation but will be further investigated. SETs on I/Os and clock lines are monitored by dedicated logic that is checking for potential I/O bank turn-offs and detections lead to a processor interruption or a reboot.

A system level watchdog is used to cover any undetected effects due to SETs.

1.4 IMPLEMENTATION RESULTS

The MCC design (without CAN interfaces) gives the following approximate utilization results after synthesis and place&route results (RT3PE3000L -1):

- Size: > 95% (with TMR and EDAC)
- System frequency: 25 MHz

The following performance figures were obtained:

- CPU: 20 Dhrystone MIPS
- FPU: 4 MFLOPS
- SpaceWire: 20 Mbit/s (twice the requirement)
- CAN: 1 Mbit/s
- SPI: 10 Mbit/s
- JTAG: 1 Mbit/s

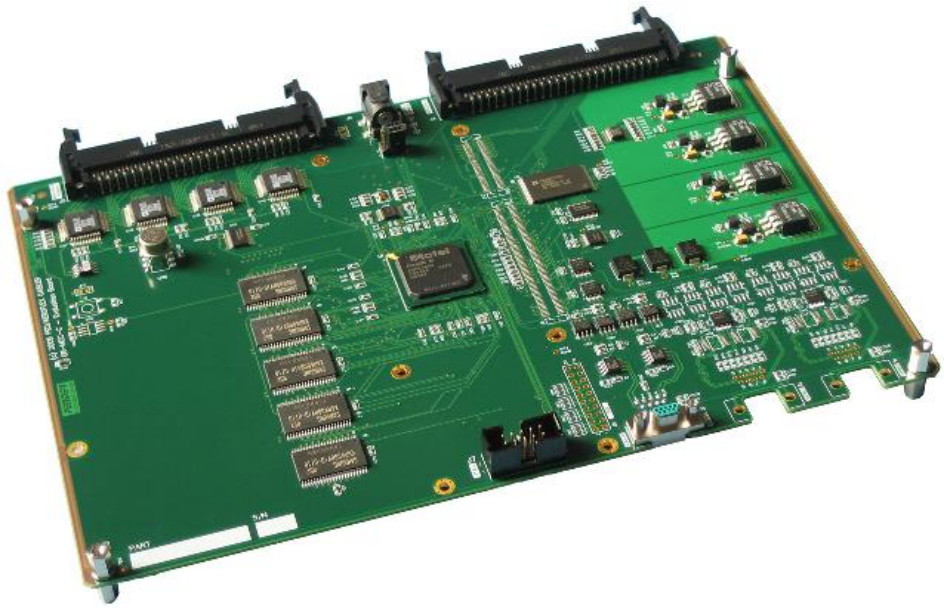


Figure: MCC-C FPGA development board

COMMUNICATION LINK IMPLEMENTATION

The system can be interfaced either via CAN or SpaceWire. The advantage of using SpaceWire links with built-in RMAP target capability is that the system can be controlled remotely, allowing upload of software to the non-volatile Flash PROM memory or directly to the volatile SRAM memory etc.

For dextrous robotic arms, wheels, masts, drills and functions needed on rovers, the approach is to use a selectively redundant CAN interface. This interface can be replaced with a single SpaceWire core without RMAP support, but with two external ports implementing automatic selective redundancy similar to the CAN approach.

For exoskeletons and applications where multiple motors are used, it is foreseen to use multiple SpaceWire links per unit that are interconnected through software or hardware routing. This allows reduction in harness for elongated structures etc. Note that the optional floating-point-unit would not fit in these configurations. There are two ways in which the links are implemented, either using two SpaceWire cores without RMAP and do the routing in software, or using a newly developed SpaceWire router [6] with two external ports and one internal port with DMA and RMAP support. The latter approach is to be implemented and evaluated in the future.

To allow flexibility and fault-containment, the Low-Voltage Differential Signaling (LVDS) buffers required for SpaceWire are implemented with off-chip parts.

CONCLUSIONS

The re-programmable RT ProASIC3 FPGA technology fits well within applications with moderate radiation requirements. The in-situ programmability enables the development of highly miniaturized systems which can be adapted to customers needs late in the development cycle. Porting a LEON3-FT system with SpaceWire links from anti-fuse to Flash-based technology went smoothly, with much of the work already performed previously for the commercial version of the IP core library.

ACKNOWLEDGEMENTS

The authors acknowledge ESA for the commissioning and funding of the development of the Motion Control Chip under ESA contract number 21737, lead by Dr. Johan Köhler. The authors also acknowledge ÅAC Microtec as the prime of the Motion Control Chip development activity.

REFERENCES

1. SpaceWire - Links, Nodes, Routers and Networks, ECSS-E-ST-50-12C
2. SpaceWire - Remote memory access protocol, ECSS-E-ST-50-52C
3. F. Bruhn et al, *"Low Temperature Miniaturized Motion Control Chip - Enabled by MEMS and Microelectronics"*, ASTRA 2008
4. S. Habinc et al., *"Using a FLASH Based FPGA in a Miniaturized Motion Control Chip"*, MAPLD 2009
5. S. Habinc et al., *"Leveraging the Availability of 32-bit Fault-Tolerant Processors Suitable for Radiation-Tolerant FPGA Devices"*, CMSE 2010
6. M. Isomäki et al., *"A Configurable SpaceWire Router VHDL IP core"*, ISC 2010