

# **A CONFIGURABLE SPACEWIRE ROUTER VHDL IP CORE**

## **SpaceWire Components (Poster)**

### **Short Paper**

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#### **ABSTRACT**

Routers are an integral part of most SpaceWire networks and many are available as discrete components or IP cores from several providers. Aeroflex Gaisler has developed a highly configurable SpaceWire router VHDL IP core to meet the needs for technology independent router designs.

The main design goals have been configurability, technology independence, support of all standardized features and expandability.

This paper will give a short overview of the basic features and focus on how the design goals have been achieved and how the resulting implementation is useful.

#### **INTRODUCTION**

Currently there are only a few SpaceWire routers available either as discrete components with a single configuration or IP cores written in a hardware descriptive language (HDL). Some lack full support for one or more features such as packet distribution and group adaptive routing.

Aeroflex Gaisler provides a library of IP cores centered around the AMBA on-chip bus [1]. This library is designed in a technology independent manner with all technology dependent modules used through technology independent wrappers if needed by the target technology.

This paper presents the design of a SpaceWire router VHDL IP core designed for the GRLIB IP library to provide a router core which is technology independent, highly configurable and provides full standard support.

#### **BASIC FEATURES**

##### **1.1 STANDARD SUPPORT AND ROUTING CAPABILITIES**

All of the optional features mentioned in the SpaceWire standard [2] are supported to some extent. The core supports all the basic features with optional header deletion and individually assignable ports for each logical address. A port equivalence register is also provided for each physical or logical address which can be used to configure the router to be able to send a packet on the determined destination port or any port mark equivalent. In other words this is an implementation of group adaptive routing.

Interval labeling is a name given to a routing table with a consecutive ranges of logical addresses going to the same port thus enabling a simpler routing table as

claimed in the SpaceWire standard. The SpaceWire router supports ranges but this does however not result in a simplified table because the core supports the more general case with any address combinations being routable to the same port of which ranges is a special case.

Another optional feature which is not commonly found in current routers is packet distribution. The core contains a register for each physical or logical address which determines that an incoming packet with a certain destination address should be distributed to additional ports.

## 1.2 CONFIGURATION

Configuration is provided through port 0 as defined in the standard. RMAP [3] reads and writes are used to access the configuration which are located at static range of RMAP addresses. An experimental implementation of the draft SpaceWire plug and play protocol [4] can also be optionally enabled. It is also accessible through port 0 but is distinguished from RMAP through the protocol ID.

The core also has the option to use an AMBA APB interface to access the configuration registers which is more efficient than sending RMAP packets through the AMBA AHB port which would otherwise be the case.

## 1.3 SWITCH MATRIX

Connecting the ports together is a switch matrix where each port can be connected to any of the other ports using wormhole routing as required by the SpaceWire standard. However, many router designs have duplicated routing tables so that destinations for incoming packets can be determined immediately without contention. The downside of this is a large area overhead since the routing table has to be duplicated once for each port.

The Aeroflex Gaisler router instead has a single routing table with pipelined access to avoid timing problems. One new destination can be determined each clock cycle and should be sufficient without any significant performance penalty with a normal workload. The case where a performance penalty would occur is when many or all ports are simultaneously sending very short packets but this scenario should be unlikely to occur at any great frequency.

## PORTS

### 1.4 SPACEWIRE PORTS

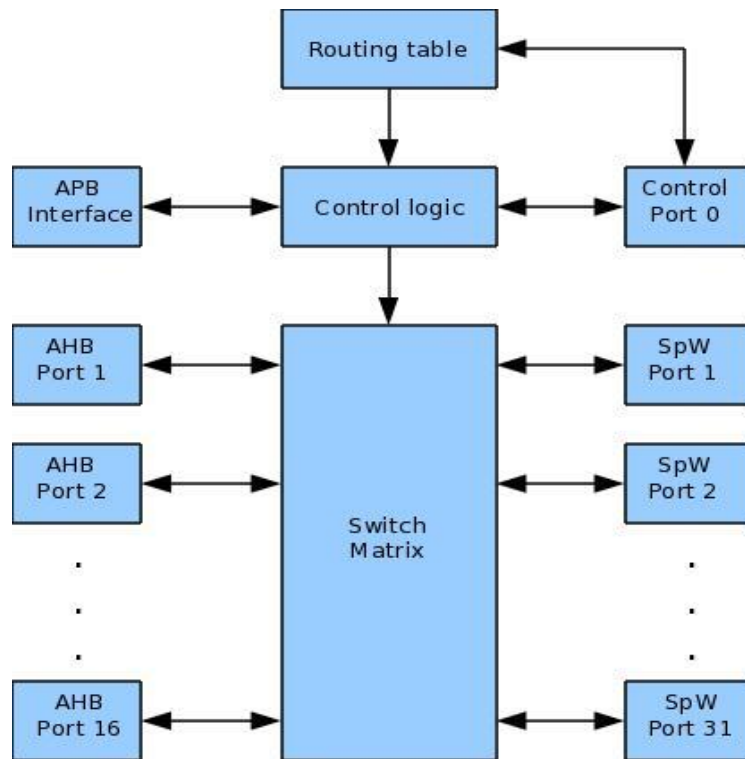


Figure 1: SpaceWire router block diagram

The total number of ports is configurable from 2 to 31. Up to 31 can be external SpaceWire ports where each port is an instantiation of the SpaceWire codec core [5] provided in GRLIB [6]. The SpaceWire codec used for the SpaceWire ports provides many different output and input physical layer implementations. Among them are self-clocking reception, sampling, SDR or DDR sampling inputs or outputs and an Aeroflex SpW transceiver interface [6]. The different interfaces each have their strong features which makes them suitable for different technologies and link speeds. This makes the core versatile in respect of technology independence.

### 1.5 AMBA AHB PORTS

Up to 16 of the ports can be DMA engines with optional RMAP targets which transfer packets on an AMBA bus of a SpaceWire network. The AMBA AHB interfaces are based on the GRSPW2 [6]. The number of ports cover the complete range of what the standard allows. Through the use of one or more AHB interfaces connected to the router ports the router can easily be expanded with existing GRLIB cores. For example MIL-1553, CAN, PCI or Ethernet cores can for example be connected to the DMA engine providing a bridge to one or more of these interfaces with a minor

amount of design work. In the same way the external parallel interface that is common in router components can be implemented.

## CONCLUSION

The Aeroflex Gaisler SpaceWire router is a highly configurable and technology independent core. It supports all of the features mentioned in the SpaceWire standard with some additional features. Due to the technology independent design and reuse of existing IP it is easy to move the design between technologies and to reconfigure a design. Due to its connection with the GRLIB IP library it can also be expanded with bridges to a wide variety of on-board buses.

## REFERENCES

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4. SpW PnP Protocol definition, Draft A v2.1, Space Technology Centre, University of Dundee, <http://spacewire.esa.int>
5. Marko Isomäki et al., “A versatile SpaceWire Codec VHDL IP Core”, International SpaceWire Conference, St Petersburg, 2010
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