INCORPORATION OF THE ESA RMAP IP CORE WITHIN MARC AND THE BEPICOLOMBO RIU

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Short Paper

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ABSTRACT

This paper describes the incorporation of the ESA RMAP IP core within the Modular Architecture for Robust Computing (MARC) system and within the BepiColombo Remote Interface Units (RIUs).

The MARC development system implemented the IP core within Actel PRO-ASIC 3E FPGAs. Both SpaceWire Initiator and SpaceWire Target configurations have been instantiated as part of the MARC project. The BepiColombo RIUs each utilise the ESA RMAP IP core configured as SpaceWire targets within Actel RTAX-S FPGAs.

The paper summarises the implementation details of each system and the performance achieved.

1. INTRODUCTION

The ESA RMAP (Remote Memory Access Protocol) IP core is a SpaceWire interface VHDL core that includes the RMAP protocol extension to SpaceWire. It has been developed with ESA funding by the University of Dundee. SEA was selected as an Alpha user of the IP core as part of the MARC development. The RMAP IP core is now currently being integrated in to the Remote Interface Units (RIUs) for the upcoming ESA BepiColombo mission to Mercury.

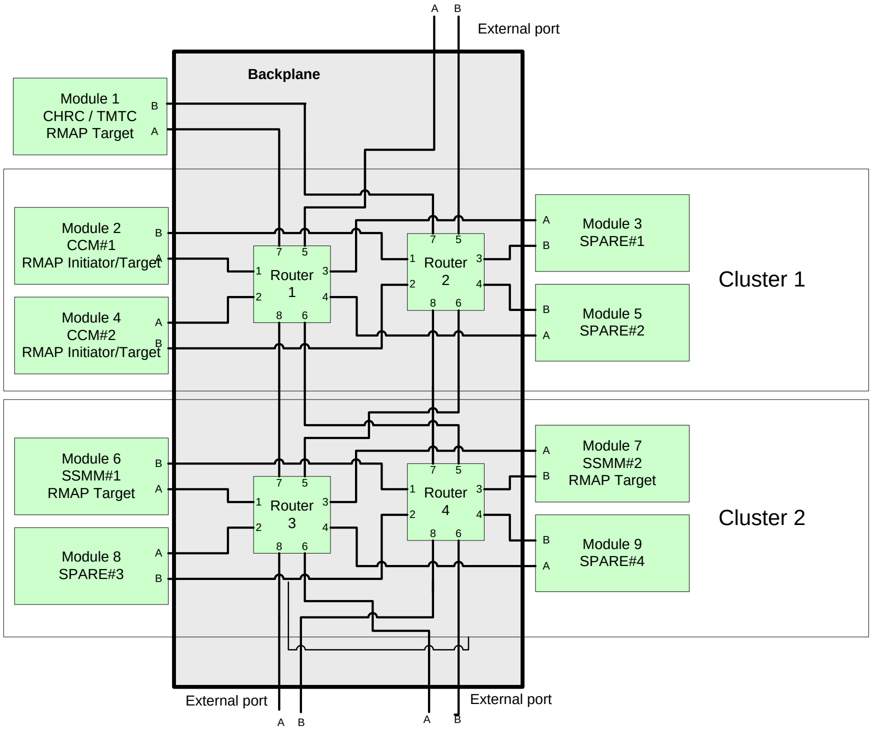
This paper begins with a review of the RMAP IP core implementations within the MARC and RIU systems, then discusses the main issues encountered during its use. Full details of the RMAP IP core can be found in the University of Dundee User Manual (reference [1]).

2. MARC IMPLEMENTATION

All MARC modules have two SpaceWire interfaces for redundancy and these incorporate RMAP functionality (via the ESA RMAP IP core). The RMAP protocol is defined within reference [2].

- The 2 core Computing Modules (CCMs) contain two full RMAP IP cores (both Initiator and Target enabled) controlled by a LEON2FT fault tolerant processor.
- The core Hardware Reconfiguration Controller (CHRC) contains two RMAP IP cores configured as Target only. This module provides the Failure Detection and Isolation functionality for the system.
- The 2 Solid State Mass Memory modules (SSMMs) contain two RMAP IP cores configured as Target only. These modules provide the bulk data storage for the system.

These modules are integrated onto an active backplane containing four Atmel AT7910E SpaceWire routers. The architecture is illustrated below.



The prime and redundant CCMs can access memory located on any module as an extension of its own memory using the RMAP protocol. The CCM can access software and data resources from at least 3 sources, i.e. local, the other CCM or the Solid State Mass Memory modules. The RMAP protocol provides an efficient memory access capability which also allows the system to recover from the failure of the prime CCM by storing context saving memory within the system which can be accessed by the redundant CCM.

3 MARC PERFORMANCE

The MARC implementation initialises the SpaceWire link at 10Mbit/s (as per reference [3]), then runs the links at 100Mbit/s. The IP core is configured in the TXCLK_DIV configuration driven by an external 100MHz clock for the Transmit clock and by a 25MHz clock for the system clock. In order to achieve the desired operational performance, the fastest -2 grade of FPGA was required. The large size of the RMAP IP core resulted in the largest ProASIC 3E device being used (3,000,000 gate A3PE3000).

Initially the RMAP IP core Initiator and Target functions were tested by direct connection of the modules to a University of Dundee SpaceWire Brick. Once the RMAP links were operational, the modules were plugged into the backplane, where testing of the SpaceWire links to/from the Atmel SpaceWire Routers was performed. At this stage the RMAP IP core Initiator was used to initiate the sending of packets from/to another RMAP IP core (Target) via the router network including self addressed packets. The only major issue encountered during this testing was a premature timeout of messages sent by the RMAP Initiator, however this has now been rectified by a later release of the IP core (v1.0).

4 RIU IMPLEMENTATION

The Remote Interface Unit has two SpaceWire Controller modules. Each module contains an FPGA containing two ESA RMAP IP cores. The Onboard Computer communicates with the RIU using SpaceWire RMAP packets to retreive sample data and command outputs. Both RMAP IP cores are configured as Target only (to ensure that no messages are initiated by the RIU). The design is targeted at an Actel RTAX2000S FPGA. The IP core is configured in the SYS_DIV configuration clocked by an external 20MHz oscillator.

5 RIU PERFORMANCE

The RIU initialises each SpaceWire link at 10Mbit/s (as per reference [3]), then runs the links at 2Mbit/s. The design has not yet been validated on the bench; however no issues are envisaged due to the relatively slow speed of the links (in relation to the previous MARC system).

6 IMPLEMENTATION ISSUES

6.1 CLOCK RECOVERY

One of the major issues experienced during integration was caused by repeated failures in the recovery of the receive clock from the SpaceWire Data and Strobe signal lines. This is a function of the SpaceWire CODEC contained within the RMAP IP core. The recovery is performed using a simple XOR gate. Numerous placements constraints were required to prevent the recovered clock from clocking the rising and falling edge input flip flops prior to their input setup time. The input XOR gate and input flip flops were manually placed within the FPGA and all VHDL blocks associated with the receive clock were constrained within a region to reduce skew. Actel have issued an application notice regarding this problem (reference [4]). A pre-synthesised core of this section would be a benefit for developers.

6.2 IP CORE EXTERNAL BUS

The external bus of the RMAP IP core can be sized as 1, 2, 3 or 4 bytes wide using a VHDL generic. The RMAP IP core is designed to increment addresses by 1 when using incrementing read/writes from memory, regardless of memory width. The addressable memory size therefore quadruples when using a 32 bit wide external bus instead of an 8 bit wide bus. There is no feature which allows the external address to increment as byte aligned i.e. Bits 1 and 0 are don’t care on a 32-bit address. This caused integration issues when passing data pointers into the RMAP Initiator from the Atmel AT697F 32 bit wide local bus which is byte aligned. This could only be resolved with a software workaround within the AT697F code.

6.3 SEU PROTECTION

A major drawback in the use of the RMAP IP core for a space mission is that SEU protection is not provided in the current RMAP IP core model. In space applications, storage elements like SRAM are susceptible to soft (transient) errors caused by heavy ions. Space grade FPGAs, such as the Actel RTAX-S provide SEU protection for the synchronous elements in the design (flip-flops); however memory blocks are not protected. Actel memory blocks can be protected using their proprietary CoreEDAC block (described within reference [5]). The RMAP IP core therefore has to be modified to incorporate CoreEDAC blocks around the RAM elements. Small memories within the IP core are implemented as flip flops.

6.4 VHDL GENERICS

The RMAP IP core contains a large amount of VHDL Generics to configure the desired functionality. VHDL Generics are contained within both the RMAP and the SpW CODEC sections of the IP core. The user therefore has to validate their own particular configuration, which is unlikely to have been previously verified. The large amount of generics impacts the results of code coverage due to the numbers of lines which are not executed.

7. SUMMARY

The RMAP IP core is a flexible, configurable VHDL IP core which can be readily adapted to meet the varied requirements of user systems. As itemised above there are a number of enhancements which could be considered for a future release to ease its usage in future space missions. Overall the integration/testing of the RMAP IP core has been positive and no issues are foreseen with the BepiColombo RIU implementation.

8. REFERENCES

[1] SpaceNet RMAP IP core User Manual Issue 1.5, 18th May 2009

[2] ECSS-E-ST-50-11C, Draft 1.3, 01 September 2008.

[3] ECSS-E-ST-50-12C, Issue 2, 31st July 2008.

[4] Actel AC305 Application Note Implementation of the SpaceWire clock recovery Logic in RTAX-S Devices

[5] Actel AC319 Application Note Using EDAC RAM for RadTolerant RTAX-S/SL FPGAs and Axcelerator FPGAs App Note